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Measurement of High-Frequency Characteristics of CNTFETs and Equivalent Circuit Model Analysis

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1. Introduction

Carbon nanotube field effect transistors (CNTFETs) are high-mobility devices that operate at very high-speeds. Theoretical analyses suggest that the cut-off frequency (f_T) of an ideal CNTFET is between 800 GHz and 1.3 THz when its gate length is 0.1 μm (1; 2). Since this frequency is much higher than that of state-of-the-art Si, GaAs, and InP transistors, CNTFETs are promising candidates for future nanoelectronic devices. Singh et al.(3) measured frequency responses of top-gated CNTFETs up to 100 MHz. Li et al.(4) observed 2.6-GHz operation of CNTFETs with an LC impedance-matching circuit. However, as Li et al. pointed out (4), measuring high-frequency performance of high-impedance devices, such as CNTFETs, is quite difficult. This is because their output impedances are much higher ($\sim 10^5$ Ω) than the impedance of the measurement system (50 Ω) using a network analyzer. To perform accurate high-frequency measurements, especially those to determine f_T values of such devices, we must measure S-parameters with a network analyzer even though large impedance mismatches hinder us from obtaining accurate measurement data. Kim et al.(5) measured S-parameters of multi-finger CNTFETs by using a network analyzer and obtained an f_T value of 2.5 GHz. They also concluded a maximum oscillation frequency ($f_{\max}$) of more than 5 GHz was obtained using the maximum stable gain (G_{msg}). Le Louarn et al.(6) obtained intrinsic f_T value of 30 GHz by measuring a CNTFET the channel of which was fabricated using dielectrophoresis to increase the CNT density. They also obtained G_{msg} value of more than 10 dB at 20 GHz.

This chapter will describe a method for accurately measuring and modeling the high-frequency characteristics of CNTFETs, with reference to our experiment and analysis (7). In the experiment, we first decreased the device impedance to be able to measure the S-parameter using network analyzer. This was achieved by developing a high-density multiple-channel CNTFET structure the output impedance of which is much lower than that of the conventional single-channel CNTFETs. Then we used a de-embedding procedure to remove existing errors in measured S-parameters of small-signal devices in order to obtain the current gain and unilateral power gain (U) that can determine accurate f_T and $f_{\max}$ values. For accurate RF modeling of CNTFETs, we developed an equivalent circuit RF model that includes parasitic resistances and capacitances of the CNTFET. Then the expression of the f_T ($f_{\max}$) was derived as a function of them. Not ignoring the higher order parasitic resistances and capacitances neglected in the cases of current RF transistors, an accurate model was obtained that can fully explain the experimental results.

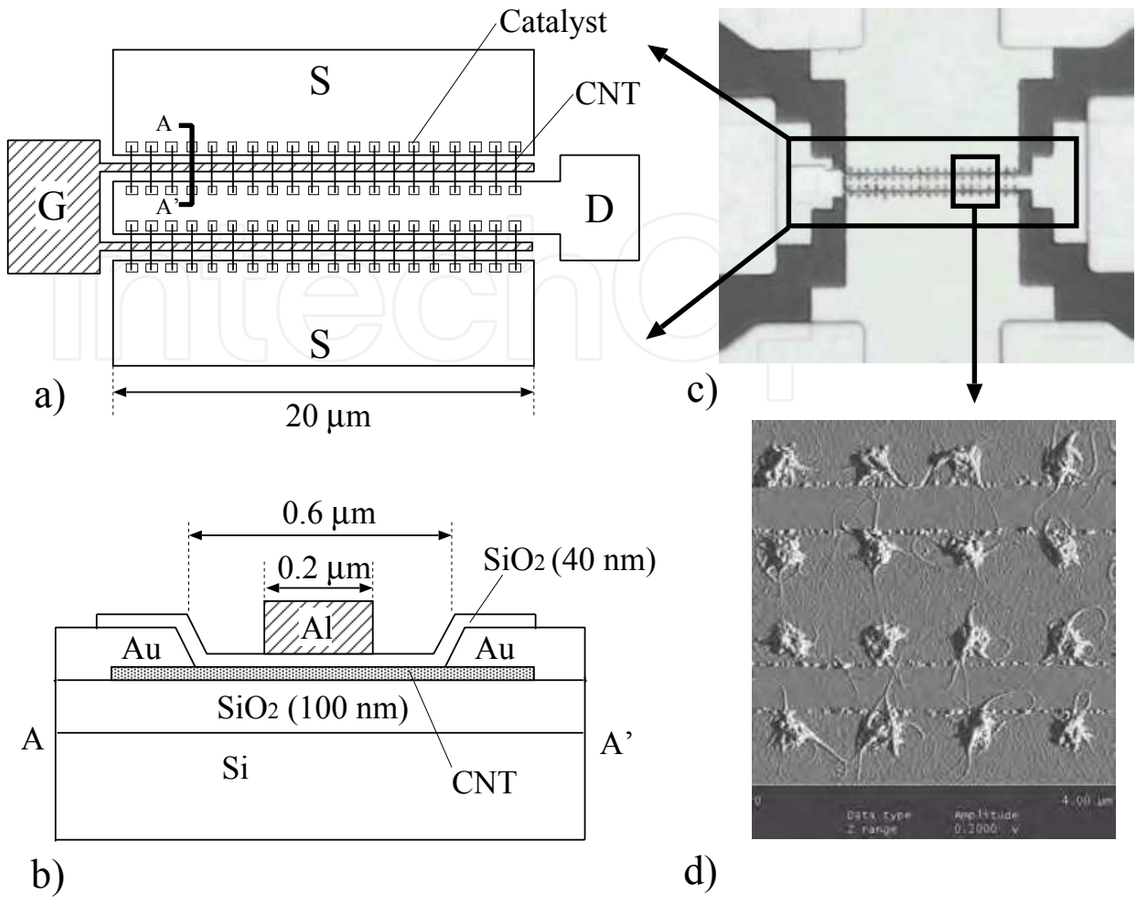

Fig. 1. Multiple-channel CNTFET structure: a) top view, b) cross section, c) optical micrograph, d) atomic force micrograph.

2. Multiple-channel CNTFET Structure

As shown in Figure 1, the evaluated CNTFET was fabricated on a SiO_2 insulator on a highly resistive (10 kΩcm) Si substrate. Iron was deposited for a catalyst and was patterned by electron-beam lithography. Single-walled carbon nanotubes (SWCNTs) were grown from the catalyst islands by chemical vapor deposition. The average density of the SWCNTs was 5 per μm, as observed in the AFM analysis (Figure 1-d). The gate oxide was 40-nm thick SiO_2, which serves as a passivation layer to retain stable characteristics and suppress hysteresis of the CNTFET I-V curve. The top-gated structure was used to reduce parasitic capacitances. The gate consisted of two 20-μm wide fingers. Thus, approximately 200 SWCNT channels were constructed in the total 40-μm gate width. The drain and source electrodes were formed by evaporation of Au, and ohmic contacts were made with CNT channels.

3. De-Embedding Procedure

Using the multiple-channel structure decreases the output impedances of the devices more than those of the single-channel CNTFETs. Therefore, their output signals can be observed

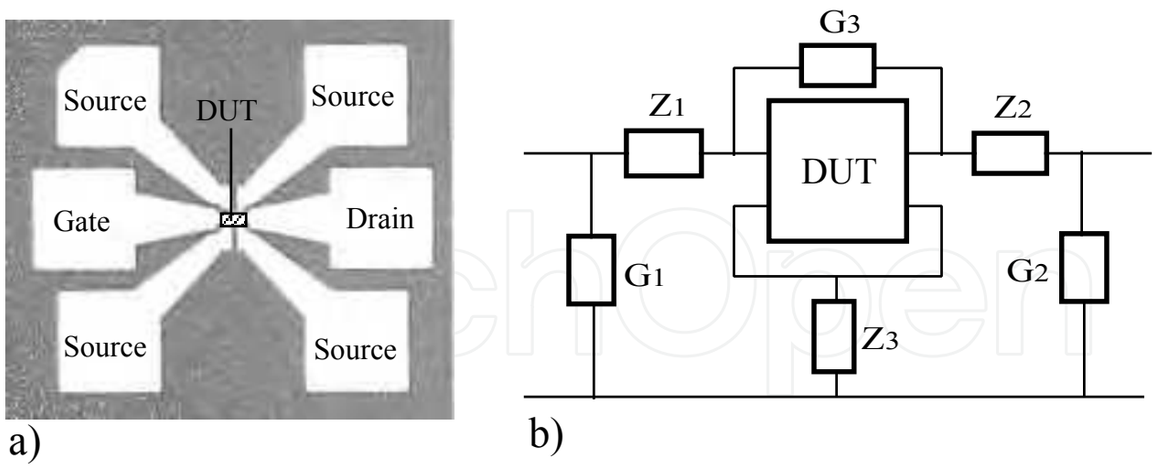

Fig. 2. RF test structure: a) pad layout, b) equivalent circuit.

directly with the network analyzer. However, output impedances of CNTFETs are still higher than those of conventional RF transistors. This means that the output signal of the device is small and easily disturbed or masked by the parasitic elements. The drain, gate, and source electrodes of the CNTFET were connected with pads for RF probe contacts. The dimensions of the pad were 100 $\times$ 100 μm, and its layout is shown in Figure 2-a. The areas of the pad and the connective wiring region are much larger than the transistor area (shown as DUT in Figure 2-a), and this large area forms parasitic elements and causes large errors in CNTFET S-parameters. Therefore, we applied the de-embedding procedure to effectively eliminate the parasitic error matrix, and only the S-parameters of the transistor were extracted using open-short-through standards on the substrate. This method is basically the same as that described in Vandamme et al.(8) and Temeijer et al.(9). The equivalent circuit of the RF test-structure, including pads and CNTFETs, is shown in Figure 2-b. In the figure, parasitic elements ($Z_1, Z_2, Z_3, G_1, G_2, G_3$) are shown. Z_1, Z_2, Z_3 are parasitic impedances, and G_1, G_2, G_3 are parasitic admittances. To determine the parasitic elements, we made four standard patterns (Open, Short1, Short2, Through) that are the same as the CNTFET measurement patterns but without CNT channels (Figure 3). The equivalent circuits of the four standard patterns are shown in Figure 4. Each standard pattern contains a different combination of the parasitic elements, and so they can be determined by the measured S-parameters of the four standards. Let us transform the measured S-parameters ($s_{ij} : i, j = 1, 2$) of the four standards to the Y-parameters and express them as $y_{ijop}, y_{ijsh1}, y_{ijsh2}, y_{ijthr} (i, j = 1, 2)$. Here, y_{ijop} is the Y-parameters of the Open standard, y_{ijsh1} is the Y-parameters of the Short1 standard, y_{ijsh2} is the Y-parameters of the Short2 standard, y_{ijthr} is the Y-parameters of the Through standard.

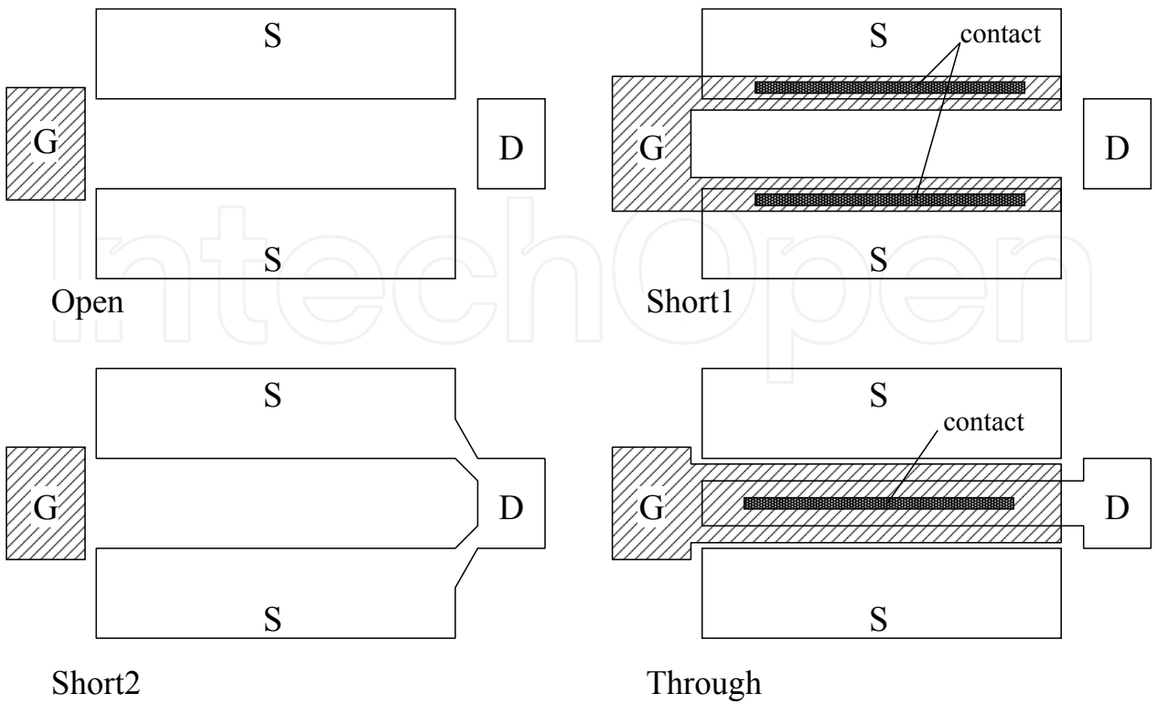

Fig. 3. Standard patterns for de-embedding

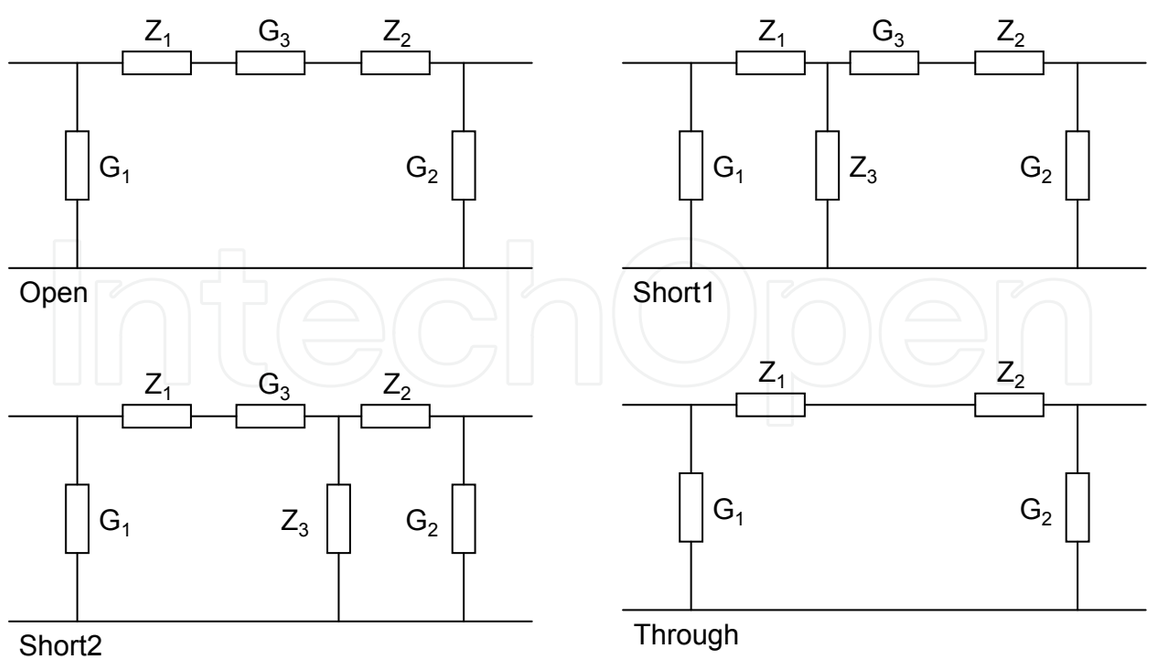

Fig. 4. Equivalent circuit of standard patterns.

Thus the parasitic elements ($Z_1, Z_2, Z_3, G_1, G_2, G_3$) can be expressed as follows:

$$G_1 = y_{11op} + y_{12op} \tag{1}$$

$$G_2 = y_{22op} + y_{12op} \tag{2}$$

$$G_3 = \left(\frac{-1}{y_{12op}} + \frac{1}{y_{12thr}} \right)^{-1} \tag{3}$$

$$Z_1 = \frac{1}{2} \left(\frac{-1}{y_{12thr}} + \frac{1}{y_{11sh1} - G_1} + \frac{1}{y_{22sh2} - G_2} \right) \tag{4}$$

$$Z_2 = \frac{1}{2} \left(\frac{-1}{y_{12thr}} - \frac{1}{y_{11sh1} - G_1} + \frac{1}{y_{22sh2} - G_2} \right) \tag{5}$$

$$Z_3 = \frac{1}{2} \left(\frac{1}{y_{12thr}} + \frac{1}{y_{11sh1} - G_1} - \frac{1}{y_{22sh2} - G_2} \right) \tag{6}$$

Using the above parasitic elements (parasitic impedance and parasitic admittance), the de-embedded matrix can be obtained by the following procedure. Let us transform the measured S-matrix ($\mathbf{S}_{meas}$) into the Y-matrix and write it as $\mathbf{Y}_{meas}$. First, we subtract G_1, G_2 from $\mathbf{Y}_{meas}$ and obtain $\mathbf{Y}_A$ as follows:

$$\mathbf{Y}_A = \mathbf{Y}_{meas} - \begin{bmatrix} G_1 & 0 \\ 0 & G_2 \end{bmatrix} \tag{7}$$

Transforming the obtained $\mathbf{Y}_A$ to the Z-matrix ($\mathbf{Z}_A$), we next subtract Z_1, Z_2, Z_3 from $\mathbf{Z}_A$ and obtain $\mathbf{Z}_B$ as follows:

$$\mathbf{Z}_B = \mathbf{Z}_A - \begin{bmatrix} Z_1 + Z_3 & Z_3 \\ Z_3 & Z_2 + Z_3 \end{bmatrix} \tag{8}$$

Again, transforming the obtained $\mathbf{Z}_B$ into the Y-matrix ($\mathbf{Y}_B$), we subtract G_3 from $\mathbf{Y}_B$ and obtain $\mathbf{Y}_{DUT}$ as follows:

$$\mathbf{Y}_{DUT} = \mathbf{Y}_B - \begin{bmatrix} G_3 & -G_3 \\ -G_3 & G_3 \end{bmatrix} \tag{9}$$

$\mathbf{Y}_{DUT}$ is the final de-embedded Y-matrix of the DUT part.

4. Measurement Results

4.1 DC Characteristics

The DC characteristics of the multiple-channel CNTFET were measured with a semiconductor parameter analyzer (Agilent 4156C). Figure 5-a shows the drain current (I_d) versus gate voltage (V_g) curve when the drain voltage (V_d) was -2 V. I_d versus V_d curve is shown in Figure 5-b. These characteristics are like p-type FETs but the drain current is not zero even when the gate voltage is small enough. This is due to the metallic carbon nanotubes. Because the metallic carbon nanotubes do not affect the high-frequency characteristics of the device, we did not perform a special removal process such as a burn out procedure. From the DC curve (Figure 5), transconductance ($g_m = \partial I_d / \partial V_g$) of 226 μS and drain conductance ($g_d = \partial I_d / \partial V_d$) of 1 mS (at V_g = 5 V, V_d = -2 V) were obtained. The drain current of our multi-channel CNTFET is more than 200 times larger than that of single-channel CNTFETs. We observed hysteresis in the I-V curves; however, the width of the hysteresis is much smaller ($\Delta V_g < 1$ V, $\Delta V_d < 0.1$ V) than that of non-passivated CNTFETs.

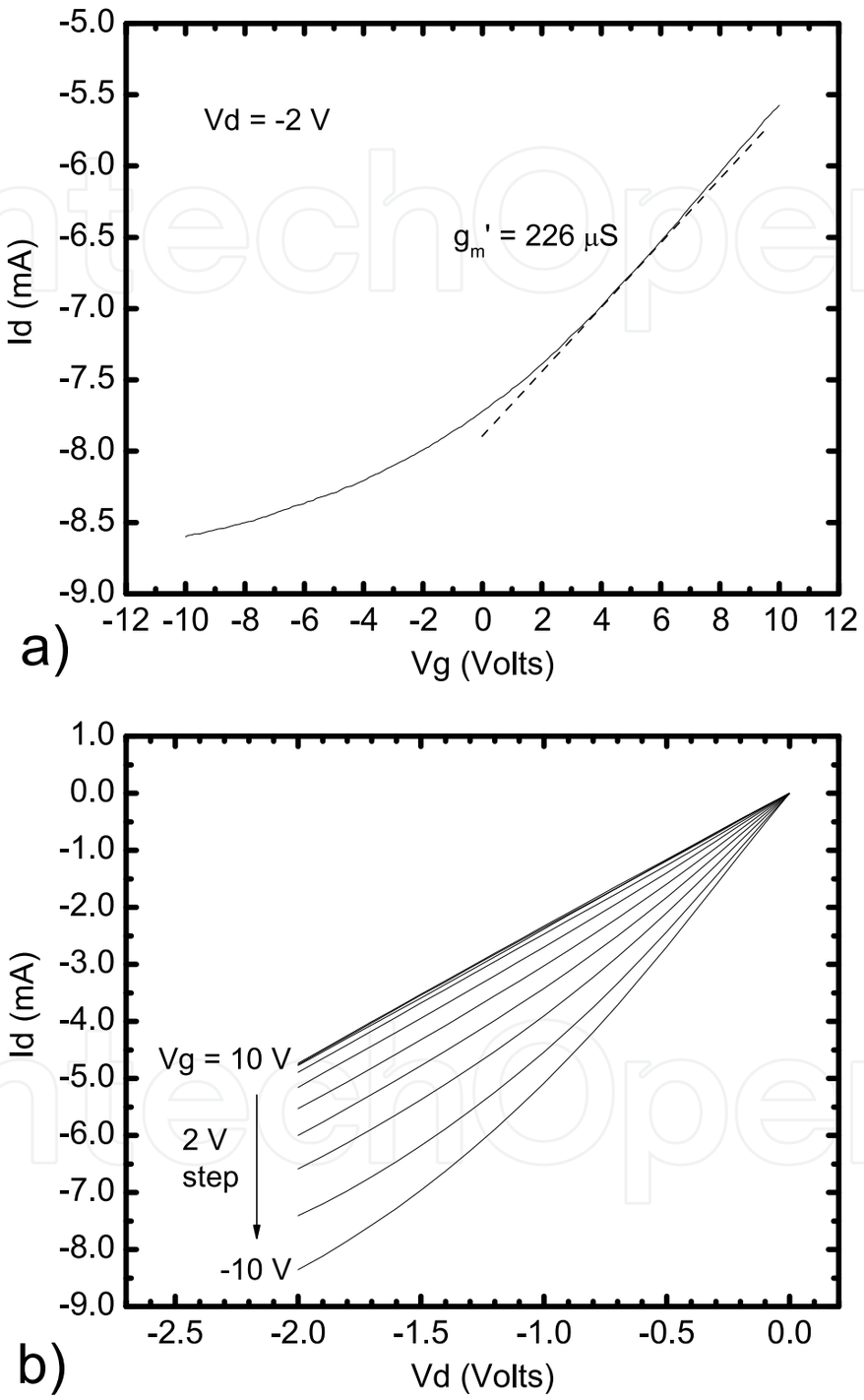

Fig. 5. DC characteristics of multiple-channel CNTFET: a) I_d-V_g curve, b) I_d-V_d curve.

4.2 RF Characteristics

Using RF probes (Cascade Microtech I40-GSG-125), we measured 2-port S-parameters of the device between 100 MHz and 20 GHz with the network analyzer (Agilent PNA N5230A). Standard SOLT-calibration was performed at the probe ends by using the calibration substrate. The measured S-parameters were de-embedded by the previously mentioned error removal procedure, and we obtained current gain ($|h_{21}| = |y_{21}/y_{11}|$) from the de-embedded Y-parameters ($\mathbf{Y}_{DUT}$) (Figure 6-a). In this figure, the measured and de-embedded data are displayed. The de-embedded data was 15 dB larger than the measured data. The f_T value was determined to be 10.3 GHz by obtaining the frequency when the current gain was unity (0 dB). Also, the unilateral power gain (U) was calculated from the de-embedded Y-parameters ($\mathbf{Y}_{DUT}$) by the formula below and plotted as a function of frequency in Figure 6-b.

$$U = \frac{|y_{21} - y_{12}|^2}{4\left[\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12})\,\mathrm{Re}(y_{21})\right]} \tag{10}$$

The $f_{\max}$ value was determined to be 3.5 GHz by obtaining the frequency when the unilateral power gain was unity (0 dB).

5. Equivalent circuit model analysis

Figure 7 shows our proposed equivalent small-signal circuit model for multiple-channel CNTFET. Here, R_s (R_d) is the resistance of the CNT between the source (drain) and gate, and contains the resistance of the CNT extensions and contact resistances. R_s and R_d were extracted from the DC measurements, as described in (10). The extracted values of R_s and R_d were 420 Ω each for our multiple-channel CNTFET. Note that R_s and R_d values of usual RF transistors are negligibly small (a few ohms); however, for CNTFETs, even when using multiple-channel structures, these resistances play a dominant role in the analysis. The g_m and g_d in Figure 7 are intrinsic transconductance and drain conductance and relate to measured transconductance (g'_m) and drain conductance (g'_d), like in Chow and Antoniadis (11), as follows:

$$g_m = \frac{g'_m}{1 - g'_m R_s - g'_d(R_s + R_d)} \quad \text{and} \quad g_d = \frac{g'_d}{1 - g'_m R_s - g'_d(R_s + R_d)}. \tag{11}$$

Using these relations and the DC measurement results, we calculated the intrinsic transconductance and drain conductance as g_m = 3.47 mS and g_d = 15.4 mS. The intrinsic g_m and g_d values are one order of magnitude larger than g'_m and g'_d because of the large R_s and R_d values. The value $C_{g-cnt}(= C_{g-cnts} + C_{g-cntd})$ is the capacitance between the gate electrode and CNTs. We assumed that $C_{g-cnts} = C_{g-cntd}$ because of the symmetry of the device. According to Burke (1), C_{g-cnt} consists of the electrostatic capacitance (C_{ES}) and the quantum capacitance (C_Q) and is given by $C_{g-cnt}^{-1} = C_{ES}^{-1} + C_Q^{-1}$. C_Q is about 100 aF/μm. C_{ES} is calculated from geometry (as shown in Figure 8-a) and is given by $C_{ES} = 2\pi\varepsilon_r\varepsilon_0/\cosh^{-1}(2h/d)$. In our case, h = 40 nm and d = 1 nm, so C_{ES} was estimated to be 42.5 aF/μm. Thus, C_{g-cnt} (one CNT) was calculated to be 30 aF/μm, and taking into account the gate length of 0.2 μm and 200 CNT channels, we calculated C_{g-cnt} = 1.2 fF ($C_{g-cnts} = C_{g-cntd} = 0.6$ fF). C_{gs} and C_{gd}, as shown in Figure 7, are parasitic capacitances between the gate and source and the gate and drain. $C_{gs} + C_{gd}$ can be approximated by the electrostatic capacitance between a coplanar stripline and ground planes on a dielectric (Figure 8-b), like in Collin (12), as follows:

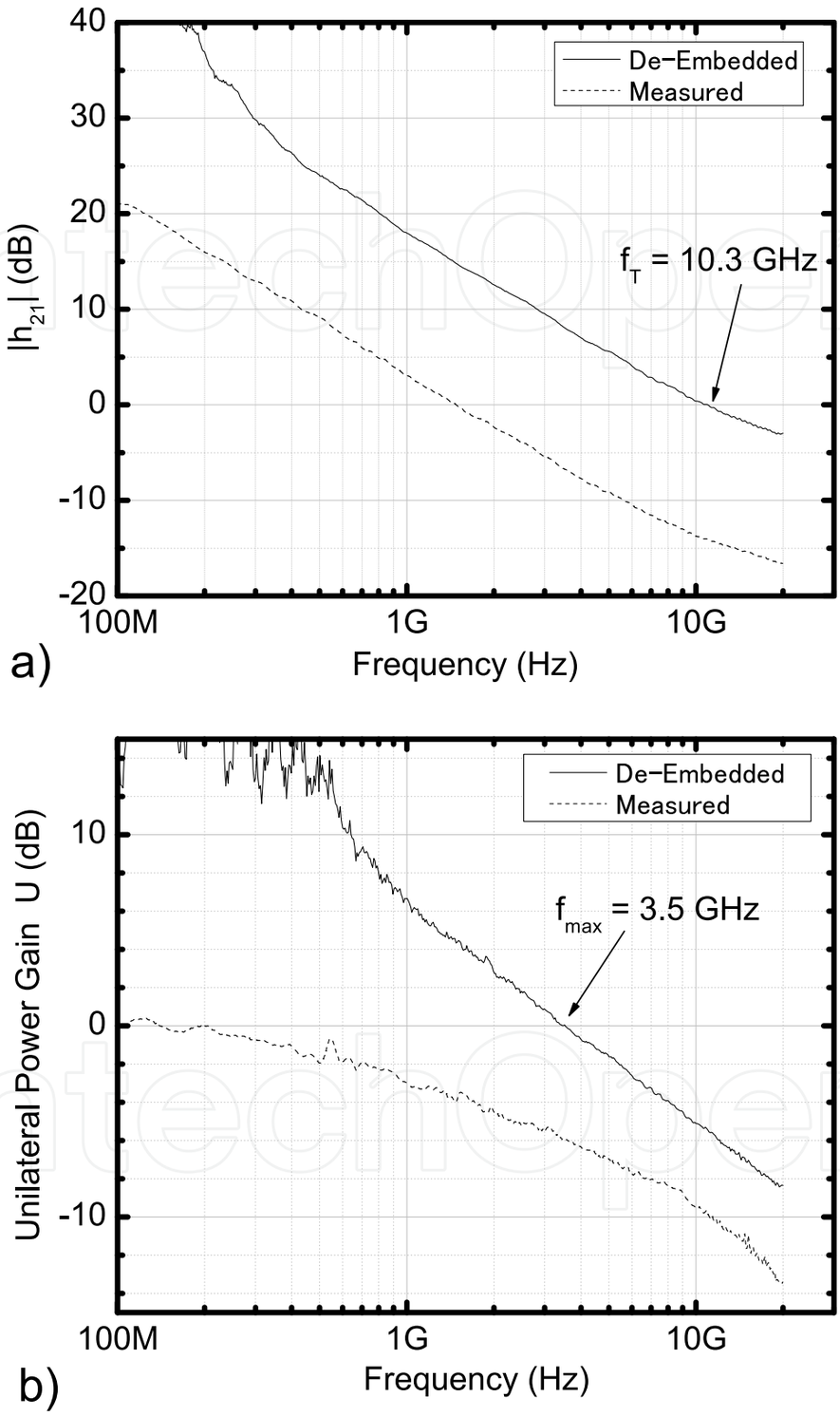

Fig. 6. RF characteristics of multiple-channel CNTFET: a) current gain ($|h_{21}|$), b) power gain (U), bias condition is $V_d = -2$ V, $V_g = 5$ V.

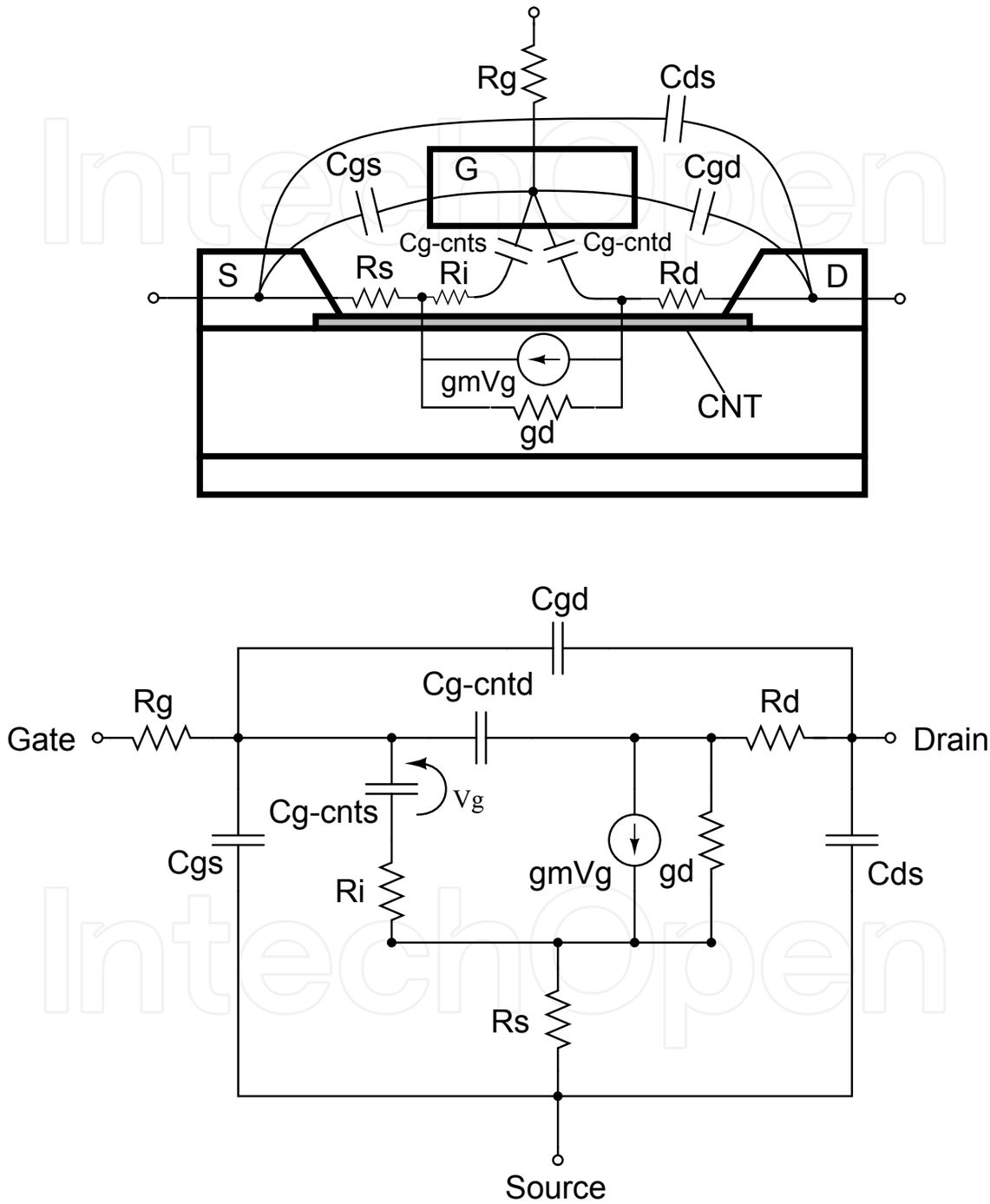

Fig. 7. Equivalent small-signal circuit model for CNTFET.

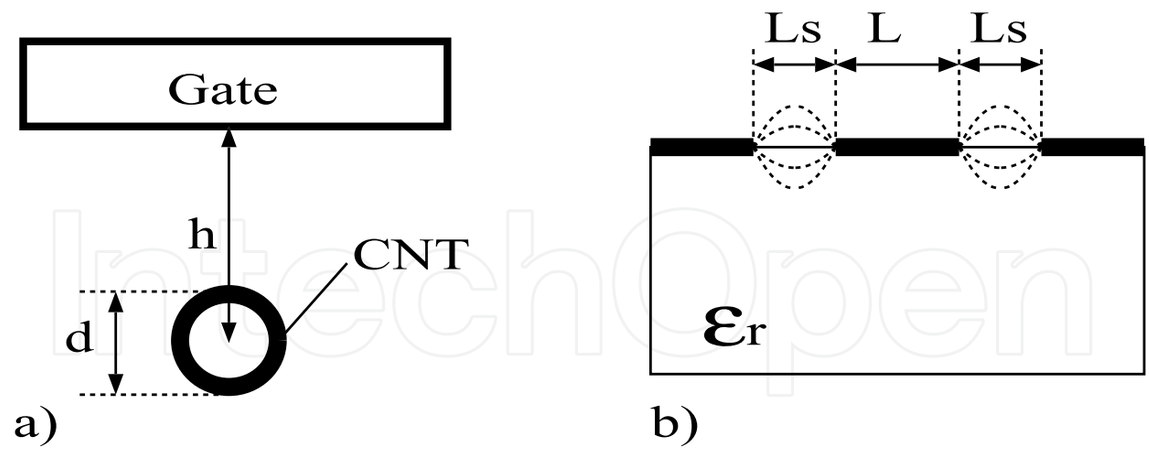

Fig. 8. Capacitance geometry: a) gate-CNT capacitance, b) coplanar stripline on dielectric

$$C_{gs} + C_{gd} = 2(\varepsilon_r + 1)\varepsilon_0 \frac{K(k)}{K(\sqrt{1-k^2})}, \tag{12}$$

where $k = L/(L + 2L_s)$, and K is the complete elliptic integral of the first kind. Considering L = L_s = 0.2 μm and W = 40 μm, we obtain $C_{gs} + C_{gd}$ = 2.2 fF.
Once the equivalent circuit model is constructed like in Figure 7, we can derive f_T by calculating the H-parameters of the circuit (13). f_T is given as

$$\frac{1}{2\pi f_T} = \frac{1}{g_m} C_g + \frac{g_d}{g_m} C_g (R_s + R_d) + C_{g-cntd}(R_s + R_d) + (C_{gs} + C_{gd})R_s, \tag{13}$$

where $C_g = C_{gs} + C_{gd} + C_{g-cnts} + C_{g-cntd}$. Substituting the parameters into Equation (13), we obtain f_T(model) = 10.6 GHz. This value is consistent with the experimental one: f_T (experiment) = 10.3 GHz.
Similarly, we can derive the expression of $f_{\max}$ by calculating the unilateral power gain U (Equation (10)) from the Y-parameter of the equivalent circuit and solving the equation: $U = 1$. The following formula is the calculation result.

$$f_{\max} = \sqrt{\frac{f_T}{2\pi R_g \left[\left(\frac{g_d}{g_m} C_g + C_{gd} + C_{g-cntd} \right) + \frac{2\pi f_T}{g_m^2 R_g} \Psi \right]}} \tag{14}$$

where C_g and Ψ are defined as follows:

$$C_g = C_{gs} + C_{gd} + C_{g-cnts} + C_{g-cntd} \tag{15}$$

$$\begin{aligned} \Psi = {} & R_s R_d \left(g_d C_{g-cnts} + g_d C_{g-cntd} + g_m C_{g-cntd} \right)^2 \\ & + R_i g_d C_{g-cnts} (C_{g-cnts} + g_d R_s C_{g-cnts} + g_d R_d C_{g-cnts} + g_m R_d C_{g-cntd}) \end{aligned} \tag{16}$$

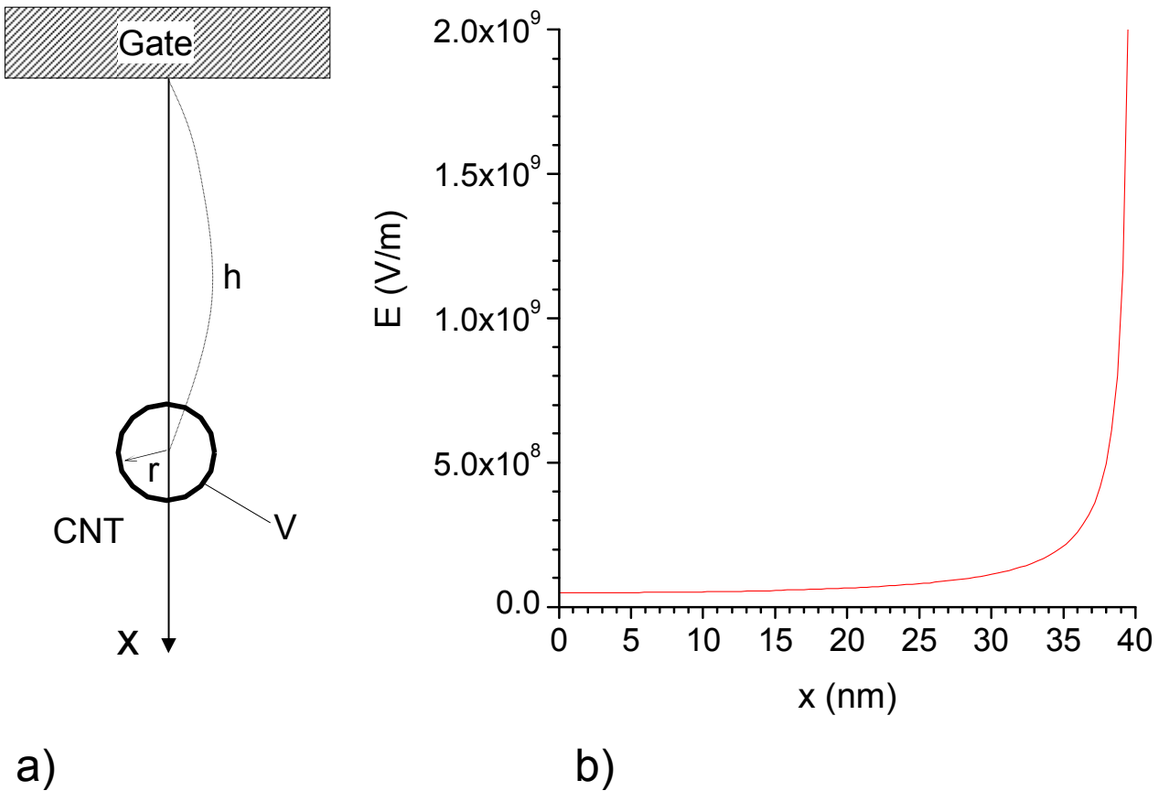

Fig. 9. (a) Geometry of gate electrode and CNT, (b) Electric field at x calculated under the condition of $V = -5$ V, $r = 0.5$ nm, $h = 40$ nm.

The above formula of $f_{\max}$ is more complicated than the expression of f_T (Equation(13)). Note that the expression of $f_{\max}$ contains not only the parameters included in the expression of f_T, but also the parameters R_g and R_i. R_g is the gate resistance and can be estimated from the resistivity of the gate electrode material of aluminum. R_g in our case is about 40 ohms. R_i is equivalent to the channel resistance (R_{ch}) in the case of current transistors and can be expressed as $R_{ch} = \alpha/g_m$. Here, α is a coefficient and has a value less than 0.2 (13). If we assume that $\alpha = 0.2$ and use the g_m of the CNTFET, we obtain $R_i \approx 60$. Using these values of R_g, R_i and the other parameters used for estimation of f_T, we can estimate $f_{\max}$ as $f_{\max}\,|_{R_i=60}$=19.2GHz. This value is much larger than the experimental value: $f_{\max}$(experiment)=3.5 GHz. To clarify this discrepancy, we should consider the phenomenon peculiar to the CNT channels, and one consistent model was proposed as shown below.

The diameter of the SWCNTs used for the multiple-channel CNTFET is about 1 nm, and S-parameter was measured under the condition that the gate electrode voltage is 5 V. This gate voltage is relatively high enough that the strong electric field exists at the vicinity of the CNTs. To estimate the electric field, we assume that the gate electrode and the CNT are an infinite conductive plane and an infinite length of conductive cylinder that is separate from the plane at the distance h and has a radius of r, as shown in the Figure 9-a. When the potential of the

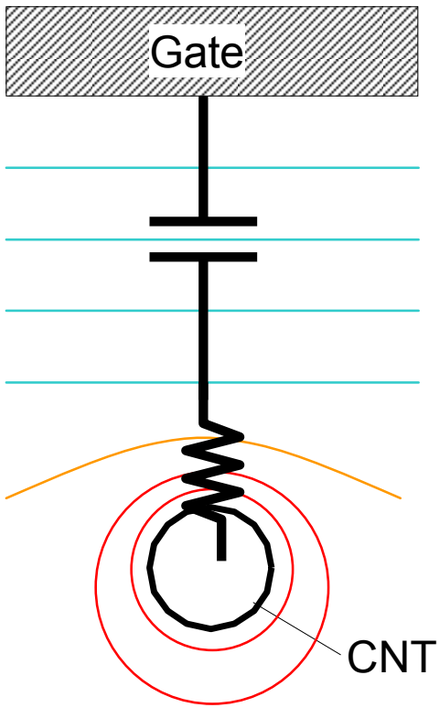

Fig. 10. Equivalent circuit between gate electrode and CNT

CNT is V, the potential at x is written as the expression below (14):

$$\phi = \frac{V}{2\cosh^{-1}(h/r)} \ln\left(\frac{x+\sqrt{h^2-r^2}}{x-\sqrt{h^2-r^2}}\right)^2 \tag{17}$$

Substituting $V = -5$ V, $r = 0.5$ nm, $h = 40$ nm (thickness of the gate oxide) to the above formula, and calculating the electric field $E = -\partial\phi/\partial x$, the result are shown in the Figure 9-b. The result shows that the electric field increases rapidly as the point is getting close to the CNT. The electric field at the CNT surface ($x = 39.5nm$) is 2.0×10^9 V/m. This means that the electric field is extremely strong at the vicinity of the CNT. In this condition, the tunneling current, Fowler-Nordheim(F-N) current, easily flows from the CNT into the gate oxide. This phenomenon is considered also in (15), and they describe that the current density of the F-N current is expressed as below:

$$J_{FN} = aE^2 \exp(-b/E) \tag{18}$$

where a and b are constants and have values $a = 2 \times 10^6 A/MV^2$ and $b = 230MV/cm$. The total F-N current that flows through all CNTs in the transistor can be described as $I = AJ_{FN}$, where A is the total area through which the F-N current flows. Let us consider the F-N current at the CNT surface ($x = 39.5nm$). In this case, the area is upper half surface of the CNT cylinder under the gate electrode. Multiplied by 200 CNT channels, the total area can be obtained as $A = 200 \cdot L \cdot \pi r$, where L is the gate length.
The variation of the potential ($\delta\phi$) corresponding to the variation of the CNT potential (δV) can be written as $\delta\phi = \frac{\partial\phi}{\partial V}\delta V$. Also the variation of the F-N current(δI) can be written as

$\delta I = \frac{\partial I}{\partial V}\delta V$. Thus, the resistance originated from the F-N current can be written as $R_{FN} = \delta\phi/\delta I = \frac{\partial \phi}{\partial V} / \frac{\partial I}{\partial V}$. Calculating R_{FN} using Equations (17) and (18), we obtain $R_{FN} \approx 75k\Omega$. Consequently, we can guess that the equivalent circuit between the gate electrode and CNT consists of the capacitance of the gate oxide and additional serial resistance(R_{FN}), as shown in Figure 10. This adds R_{FN} to R_i in our equivalent circuit model of the CNTFET, so that we can write $R_i = R_{ch} + R_{FN} = 60 + 75k \approx 75k\Omega$. Substituting this into Equation (14), we obtain $f_{\max}$(model)=3.4 GHz. This $f_{\max}$ value is very near to the experimental value: $f_{\max}$(experiment)=3.5 GHz.
From the above discussion, we get a guideline to improve the high-frequency characteristics of the CNTFET. To increase the f_T, the parasitic capacitances ($C_{gs} + C_{gd}$) and the resistances ($R_s + R_d$) need to be reduced. If ($C_{gs} + C_{gd}$) and ($R_s + R_d$) are negligible, then Equation (13) becomes $f_T = g_m/2\pi C_{g-cnt}$, and we obtain $f_T \approx 460$ GHz. The parasitic resistance R_s (R_d) is the resistance of CNT extensional part between the source (drain) electrode and the channel. A candidate to decrease this resistance is doping (16). To improve the value of $f_{\max}$, R_g and $R_i(R_{FN})$ should be decreased in addition to reducing the parasitic capacitances and resistances. Because R_{FN} originates from the strong electric field near CNTs, as discussed above, we should develop a CNTFET that operates with low gate voltages.

6. Summary

This chapter described a method for accurately measuring and modeling the high-frequency characteristics of CNTFETs. To directly measure using a network analyzer, we developed a high-density multiple-channel CNTFET structure the output impedance of which is much lower than conventional single-channel CNTFETs. We also focused on accurately measuring S-parameters, e.g., we used a de-embedding procedure that removes existing errors in measured S-parameters of high-impedance devices. Consequently, we obtained a cut-off frequency (f_T) of 10.3 GHz and a maximum oscillation frequency ($f_{\max}$) of 3.5 GHz. We also proposed an equivalent circuit RF model that includes the higher order parasitic resistances and capacitances that are neglected in the case of current RF transistors. The model, therefore, can explain the experimental results very accurately. The analysis also revealed that decreasing the parasitic capacitances of the electrodes and the resistances of the CNT extensions greatly improves the high-frequency performance of CNTFETs.

7. References

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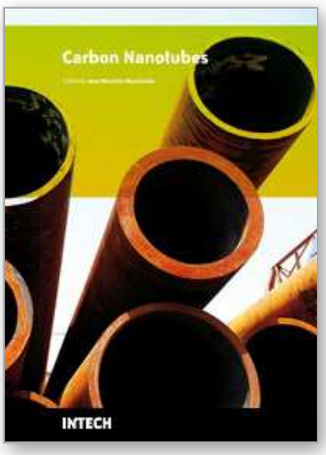

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This book has been outlined as follows: A review on the literature and increasing research interests in the field of carbon nanotubes. Fabrication techniques followed by an analysis on the physical properties of carbon nanotubes. The device physics of implemented carbon nanotubes applications along with proposed models in an effort to describe their behavior in circuits and interconnects. And ultimately, the book pursues a significant amount of work in applications of carbon nanotubes in sensors, nanoparticles and nanostructures, and biotechnology. Readers of this book should have a strong background on physical electronics and semiconductor device physics. Philanthropists and readers with strong background in quantum transport physics and semiconductors materials could definitely benefit from the results presented in the chapters of this book. Especially, those with research interests in the areas of nanoparticles and nanotechnology.

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