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Behavioral Modeling of Flash Memories

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1. Introduction

Over the past ten years, the interest in the development of accurate and efficient models of high-speed digital integrated circuits (ICs) has grown. The generation of IC models is of paramount importance for the simulation of many advanced electronic applications. IC models are used in system level simulation to predict the integrity of the signals flowing through the system interconnects and the switching noise generated by the current absorption of the circuits, that can interfere on the stable functioning of the entire system.
In this scenario, the common modeling resource is based on the detailed description of the IC functional behavior obtained from the information on the internal structure of devices and on the their physical governing equations. These models, however, are seldom available since they disclose proprietary information of silicon vendors. In addition they turn out to be extremely inefficient to handle the complexity of recent devices and demand for the availability of simplified models. Owing to this, the most promising strategy is the generation of the so-called behavioral models or macromodels, that mimic the external behavior of a device and that can be obtained from external simulations or measurements.
A typical example of devices that strongly demand for the availability of reliable behavioral models is represented by the class of digital memories, that are widely used in modern electronic equipments and that are often provided by external suppliers along with low-order or partial models only. The modeling of the power delivery network of ICs is addressed in (ICEM, 2001; Labussiere-Dorgan et al., 2008; Stievano et al., 2011b) and the modeling of I/O ports in (Stievano et al., 2004; Mutnury et. al., 2006; IBIS, 2008; Pulici et al., 2008; Cao and Zhang, 2009; Stievano et al., 2011a). In these contributions most of the efforts are made to define and improve the model structures and to provide general modeling guidelines for the computation of model parameters from both numerical simulations and real measurements.
The aim of this chapter is to provide a unified modeling framework for the combined application of state-of-the-art techniques to the generation of behavioral models of digital ICs from numerical simulation and real measured data. All the results presented in this study are based on a 512Mb NOR Flash memory in 90 nm technology produced by Numonyx, which is representative of a wide class of memory chips.

2. Macromodel description

This section focuses on the classification of the external ports of a Flash memory and on the available resources for the modeling of its external behavior.

2.1 Classification

The schematic of Fig. 1, represents the typical structure of packaged memory chips in stacked configuration. These devices are composed of a number of silicon dies encapsulated within the same package and connected through bonding wires to the package pads as shown in the example structure. For a single memory chip like the die #1 in the figure, the external pads allowing the chip to communicate to the external circuitry can be classified into three classes:

(*a*) the VDD*n* and VSS*n* pads, corresponding to the core power delivery network of the memory that carries the energy to the memory matrix, the digital circuitry and possible additional analog blocks within the die;

(*b*) the DQ*n* pads, corresponding to the high-speed I/O buffers;

(*c*) the VDDQ*n* and VSSQ*n* pads, corresponding to a dedicated power structure, i.e., the so-called power rail, that consists of two on-chip traces connecting the supply pads and supplying the I/O buffers. A limited number of buffers (in general from one to four) is supplied by two adjacent VDDQ*n* and VSSQ*n* pads;

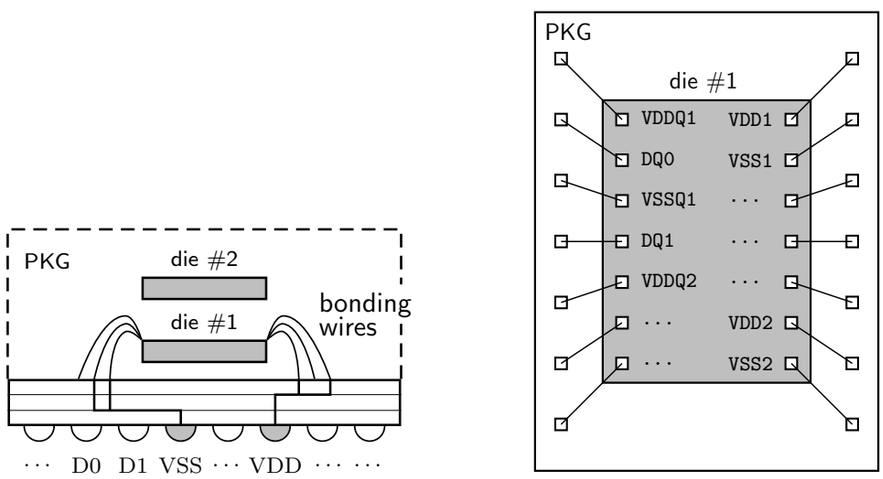


Fig. 1. Typical structure of a memory chip (i.e., the die #1) encapsulated in package. Left panel: side view; right panel; top view.

It is important to remark that the structure of Fig. 1 provides an exemplification aimed at classifying the ports and the behavior of a memory. Some minor differences might exist and depend on the specific device at hand. However, possible differences do not change the above classification and the proposed modeling methodology.

Based on the previous classification, a memory macromodel is a multiport equivalent describing the port behavior of the electrical voltage and current signals at die pads. Also, due to the inherent internal structure of this class of devices, the macromodel can be decomposed into the following submodels.

(*a*) a dynamical model for the **core power delivery network** that reproduces the port constitutive relation of the multi-terminal circuit element defined by the VDD*n* and VSS*n* pads.

(*b*) a set of dynamical models for the **I/O buffers** that include the effect of their dedicated power supply structure and that describe the port constitutive relations of the three terminal circuit elements defined by the DQ*n*, VDDQ*n* and VSSQ*n* pads.

(c) a dynamical model for the VDDQn and VSSQn **power rail** network.

It is worth noticing that in many practical cases, the above submodels can be assumed independent one to each other since the possible coupling among the three physical structures turns out to be extremely low and can be neglected. As an example, this has been verified by a set of on-chip measurements carried out on the same memory IC considered in this study (see Fig. 2).

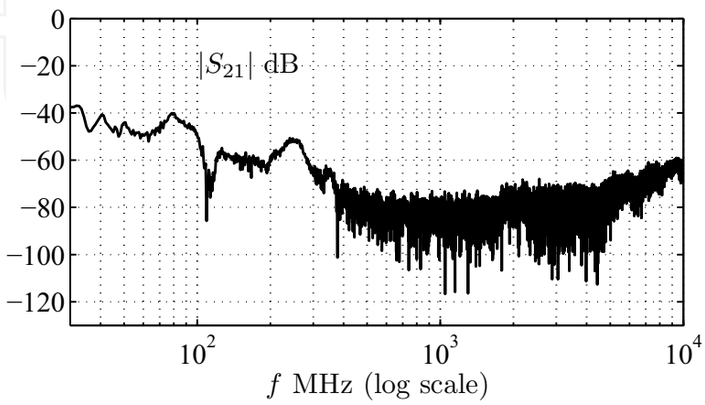


Fig. 2. On-chip measurement of the S21 scattering parameter carried out between two heterogeneous pairs of VDDn-VSSn and VDDQn-VSSQn supply pads. The measurement highlights the low coupling between the core and the buffer power delivery networks for the example test chip considered in the study.

2.2 Core power delivery network

According to (Stievano et al., 2011a;b), the model for the core power supply of ICs is defined by a simplified - physically inspired - circuit equivalent that attempts to describe the different blocks involved in the power delivery network of a digital IC. A common assumption in these approaches is the description of the core power delivery network of the IC by means of a Norton equivalent like the one of Fig. 3*a*, where the short-circuit current generator $A(s)$ accounts for the internal switching activity of the device and the equivalent impedance $Z_e(s)$ accounts for the passive interconnect structure and body diodes. This assumption holds when the physical dimension of the silicon die and the frequency bandwidth of interest are compatible with lumped modeling. When these conditions are met, this simplification is the best solution to estimate the model parameters from external measurements. In the state-of-the art modeling resources, the simple Norton equivalent of Fig. 3*a* can be complemented by possible additional passive circuit elements guessed from some information on the internal structure of the IC.

The estimation of the model parameters of the Norton equivalent amounts to computing the short-circuit current source via the transient measurement or simulation of the current drawn by the IC core during normal operation and the short-circuit admittance via frequency-domain measurements (e.g., via the scattering parameter responses of the VDD-VSS structure). It goes without saying that the frequency-domain measurements do not directly provide a computational model that can be directly used in a simulation environment like SPICE. Experience, supported also by the evidence that the die is electrically small, teaches us that the interpretation of $Z_e(s)$ and its conversion into an equivalent circuit is rather straightforward.

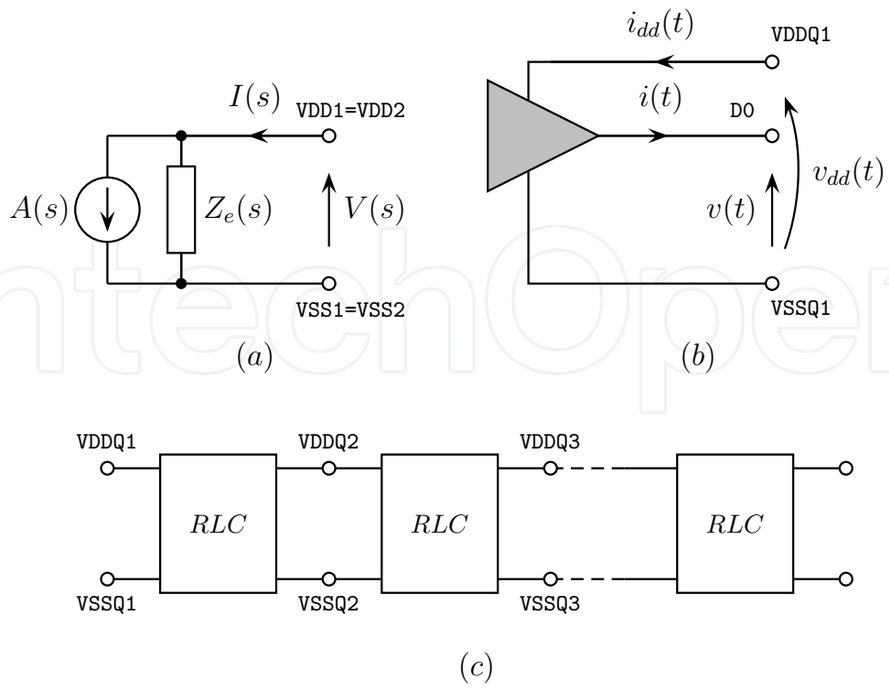


Fig. 3. Model structures: (*a*) Norton equivalent for the VDD-VSS core power delivery network; (*b*) nonlinear dynamical model for the I/O buffers (e.g., the DQ0 pad of Fig. 1); (*b*) cascade lumped equivalent of the power rail.

2.3 I/O buffers

Different approaches are used to obtain behavioral models of the I/O ports of a digital IC. The most common approach is based on simplified equivalent circuits derived from the internal structure of the modeled devices. This approach leads to the I/O Buffer Information Specification (IBIS, 2008; Pulici et al., 2008), which is widely supported by electronic design automation tools and dominates modeling applications. However, the growing complexity of recent devices and their enhanced features like pre-emphasis and specific control circuit, demand for refinements of the basic equivalent circuits. In order to facilitate the modeling of these features, alternate methodologies based on the estimation of suitable parametric relations have been proposed (Stievano et al., 2004; Mutnury et. al., 2006). These methodologies are aimed at reproducing the electrical behavior of device ports (see Fig. 3*b*), without any use of physical insights and of equivalent circuit representations. The advantage of these approaches relies in the flexibility of the mathematical description of models with respect to the circuit representation and on the computation of model parameters from the responses recorded at the device ports only. Furthermore, the parametric approaches offer simple and well-established procedures for the estimation of model parameters from real measured data.

For the case of output buffers, the common assumption in the current state-of-the-art solutions is the description of the port electrical behavior of the circuit via the following two-piece relation:

$$\begin{aligned} i(t) = {} & w_H(t) i_H(v(t), v_{dd}(t), \tfrac{d}{dt}v(t), \tfrac{d}{dt}v_{dd}(t), \tfrac{d^2}{dt^2}\ldots) + \\ & w_L(t) i_L(v(t), v_{dd}(t), \tfrac{d}{dt}v(t), \tfrac{d}{dt}v_{dd}(t), \tfrac{d^2}{dt^2}\ldots) \end{aligned} \tag{1}$$

where v, v_{dd} and i are the buffer output and power supply port voltage and current variables, with associated reference directions, w_H and w_L are switching signals accounting for the device state transitions and i_H and i_L are nonlinear dynamical relations accounting for the device behavior in the fixed high and low logic states, respectively. A similar relation holds for the power supply current and a simplified model structure, that can be considered as a subclass of eq. (1), can be adopted for the alternate case of input ports. The readers should refer to (Stievano et al., 2004) for additional details.
The estimation of model (1) amounts to computing the parameters of submodels i_H and i_L and the weighting signals w_H and w_L from suitable port transient responses.

2.4 Power rail

As outlined in the introduction, the power rail supplying the I/O buffers consists of two on-chip coplanar metallic traces connecting the VDDQn the and VSSQn pads, that have a non negligible size and that are regularly distributed along the rail (see Fig. 1). Owing to this, a simple transmission line model for coplanar structures can be hardly used. Instead, a model structure like the one of Fig. 3*c*, that consists of the cascade connection of lumped blocks, is more suitable for the description of the rail and allows the computation of model parameters from external measurements and simulations.

3. Model estimation by simulation

This section briefly outlines the resources for the generation of a memory macromodel from the simulation of detailed numerical models of devices.
When simulation models based on the governing equations describing the behavior of a memory are available, the estimation of the parameters of the submodels of Fig. 3 is a standard procedure. State-of-the-art techniques are ready to be used for the computation of model parameters.
For the core power delivery network, transient and frequency-domain simulations can be processed for the computation of the short-circuit current and of the equivalent impedance of the Norton equivalent of Fig. 3. Readers are referred to (ICEM, 2001) for additional details. It is also important to remark that when the structure of a device is known, even possible different model structures can be effectively used.
Similar comments apply to the power rail structure. Also for this case, frequency-domain 3D EM simulations of the power structure can be used for the fitting of the parameter of a circuit equivalent, like the one of Fig. 3*c*.
On the other hand, I/O buffer models, either defined by simplified equivalent circuits or by black-box mathematical relations, can be obtained via the procedure suggested by IBIS (IBIS, 2008) and collected in (Stievano et al., 2004; Mutnury et. al., 2006), respectively .

4. Model estimation by measurements

This section summarizes the procedure for the estimation of the models shown in Fig. 3 from measurements. In this work a special emphasis is given on the model generation from measured data since this procedure is less established and possible difficulties in the computation of model parameters from experimental data worth to be highlighted and discussed.

4.1 Core power delivery network

The generation of the Norton equivalent of the core power delivery network requires the estimation of the equivalent impedance and of the short-circuit current source of Fig. 3*a*.

Short-circuit current source. The computation of the current source is the most critical step of the modeling process and special care must be taken in collecting, interpreting and processing the measured data. From a theoretical point of view, the determination of the A term would require the measurement of the current flowing through ideal short-circuits terminating the core power supply pads on the right panel of Fig. 1 (i.e., the VDDn and VSSn pads). However, in practice, the pads cannot be shortened and the circuit operation of the die must be assessed with the device encapsulated in a package and mounted on a board. Figure 4 shows the equivalent circuit, in the Laplace domain, of the setup for the external measurement of the switching current I_{SS}.

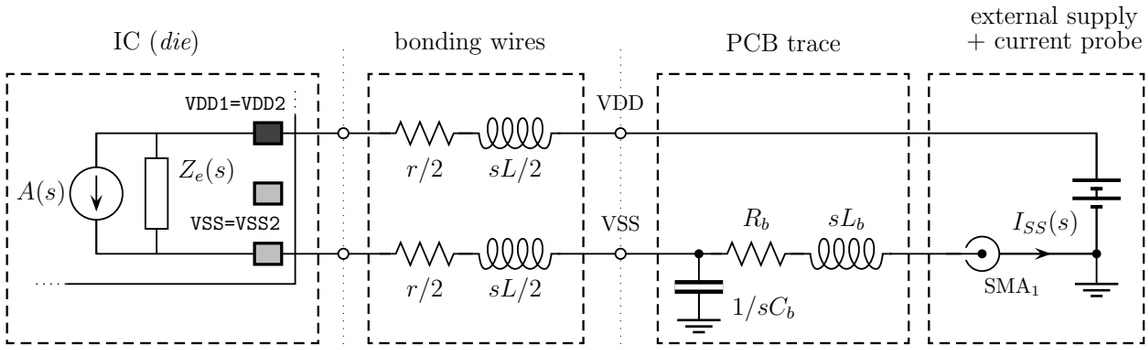


Fig. 4. Simplified equivalent of the setup used for the measurement of the equivalent impedance of the core power delivery network and the short-circuit switching current of a digital IC.

In the scheme of Fig. 4 the external power supply provided by a voltage regulator and a possible shunt capacitance is simply represented by an ideal battery connected to the VDD ball. The VSS ball is connected to a SMA connector via an on-board trace, that is represented by a lumped equivalent in Fig. 4. The transient current $i_{ss}(t)$ is obtained via an indirect measurement of the voltage drop across a R=1 Ω resistor mounted on the connector SMA$_1$. This method, following the standard for the measurement of the conducted emission of ICs in the range from dc to 1GHz (IEC61967, 2006), has been selected among a limited number of possible alternative techniques, since it is simple to implement and has proved to demonstrate accurate results in practical applications (Fiori & Musolino, 2003).
Once the switching activity current $i_{SS}(t)$ is recorded, the measured waveform needs to be suitably processed for de-embedding the effects of the measurement setup. The readers should refer to (Stievano et al., 2011a) for additional details and a more comprehensive discussion of the post-processing for the same example test chip of this work.

Equivalent impedance. The estimation of the equivalent impedance $Z_e(s)$ is obtained from the scattering frequency-domain measurements of the core-power delivery structure of Fig. 1. This can be done by using the same setup of Fig. 4 from the S_{11} measurements of the scattering parameter response of the structure seen from the connector SMA$_1$ with and without the IC mounted on it. The measured data is converted into the impedance representation

$$Z_{11} = R_0 \frac{(1 + S_{11})}{(1 - S_{11})} \tag{2}$$

where $R_0 = 50\,\Omega$ is the reference impedance of the VNA. The values of the circuit equivalent of Fig. 4 are then estimated via simple fitting from Z_{11}. Briefly speaking, the above fitting is achieved by means of the following two step procedure:

- Measurement of S_{11} without the IC mounted on the board and computation of the values of the R_b, L_b and C_b elements;
- Measurement of S_{11} with the IC mounted on the board and computation of the remaining parameters values r, L and network response $Z_e(s)$.

Test board. Figure 5 shows the board designed for the measurement required by the proposed modeling methodology. The board implements the basic features required by the ideal setup of Fig. 4. It is composed of a general purpose control circuitry for the operation of the device under test, and of a measurement board holding the IC under test and the measurement fixture. The measurement board is connected to the control board via a pair of 40-pin QTE connectors, and can be replaced to test different ICs. The memory controller, implemented in a FPGA, has been designed to allow the memory to operate at 66MHz and perform repeatedly the basic cycles (*program, erase, read*).

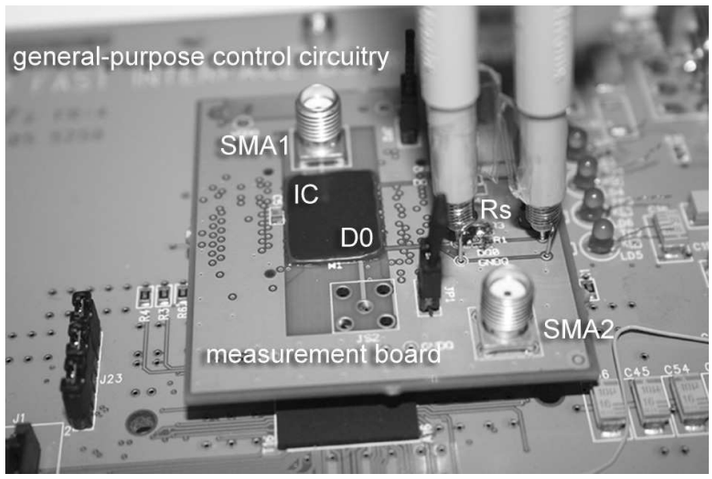


Fig. 5. Measurement board for recording the core switching activity current for the example IC.

The indirect measurement of the transient current via the voltage drop on series resistors mounted on the connector SMA_1 was carried out with a LeCroy WavePro 7300A scope (3 GHz bandwidth, 10 GS/s). To reduce the effects of the measurement noise, the memory buffers have been forced to produce a periodic bit pattern and the averaging feature of the scope has been set (16 waveforms were considered for the average). As an example, Figure 6 shows a slice of the measured transient current $i_{ss}(t)$ observed during a complete operation phase.
The frequency domain scattering measurements for the computation of the Norton equivalent impedance has been carried out via a Agilent Vector Network Analyzer (VNA) E5071B (300 kHz to 8.5 GHz). As an example, Fig. 7 shows the impedance seen by the connector that has been recorded with and without the IC mounted on the board. This Figure also compares the measurements with the responses of the lumped simplified equivalent circuits of Fig. 4 that has been estimated via simple fitting. The measured transfer functions in Fig. 7 shows some spurious resonances in a frequency region above 200 MHz that does not need to

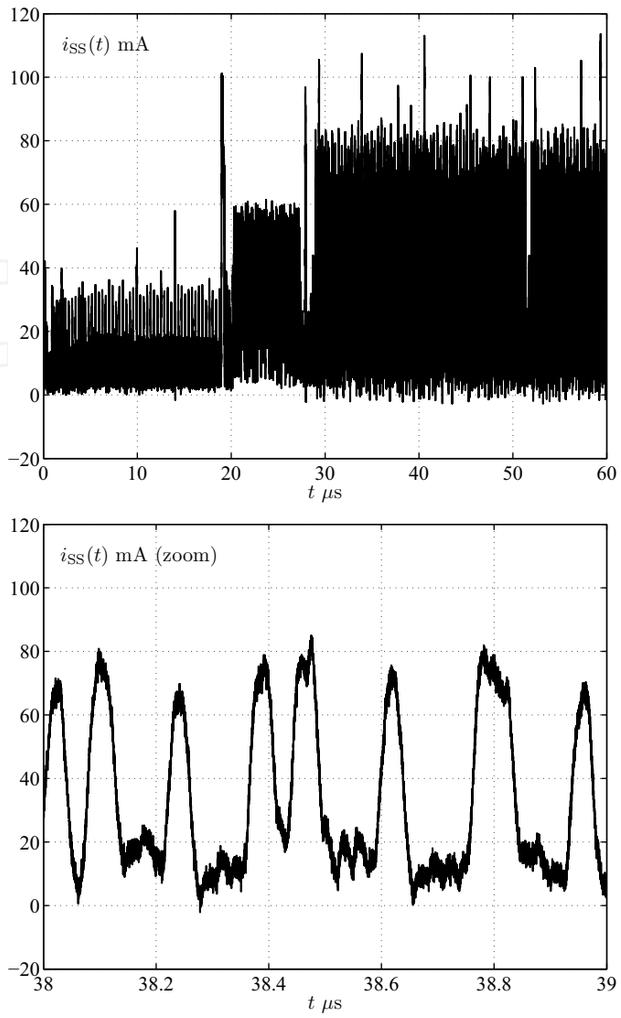


Fig. 6. Measured transient current $i_{SS}(t)$ carried out on the example commercial memory chip.

be modeled by a lumped equivalent accounting for the behavior of the IC. These effects are determined by the test fixture and by the package, and do not belong to the supply structure of the silicon device, that is generally dominated by a smooth capacitive behavior.
It is worth noticing that the on-chip probing, when available, is a good alternative option to collect measured data that can be readily converted into the admittance representation (an example of such test strategy is available in (Stievano et. al., 2009), where partial results are available for the same test vehicle considered in this study). In this work, the measurements have been carried out by means of a CascadeMicrotech probing station and a Agilent vector network analyzer. The two-port responses are obtained via Signal-Ground (SG) probes, with the G contact connected to the reference pad of the port. The power supply is provided to some die pads via DC and RF probes to mimic the actual biasing conditions. An example of the measurement setup is shown in Fig. 8.
Figure 9 shows a selection of two-port measured scattering responses of the VDD-VSS network of Figure 1 compared to the responses of a simple lumped equivalent $Z_e = 1/sC$.

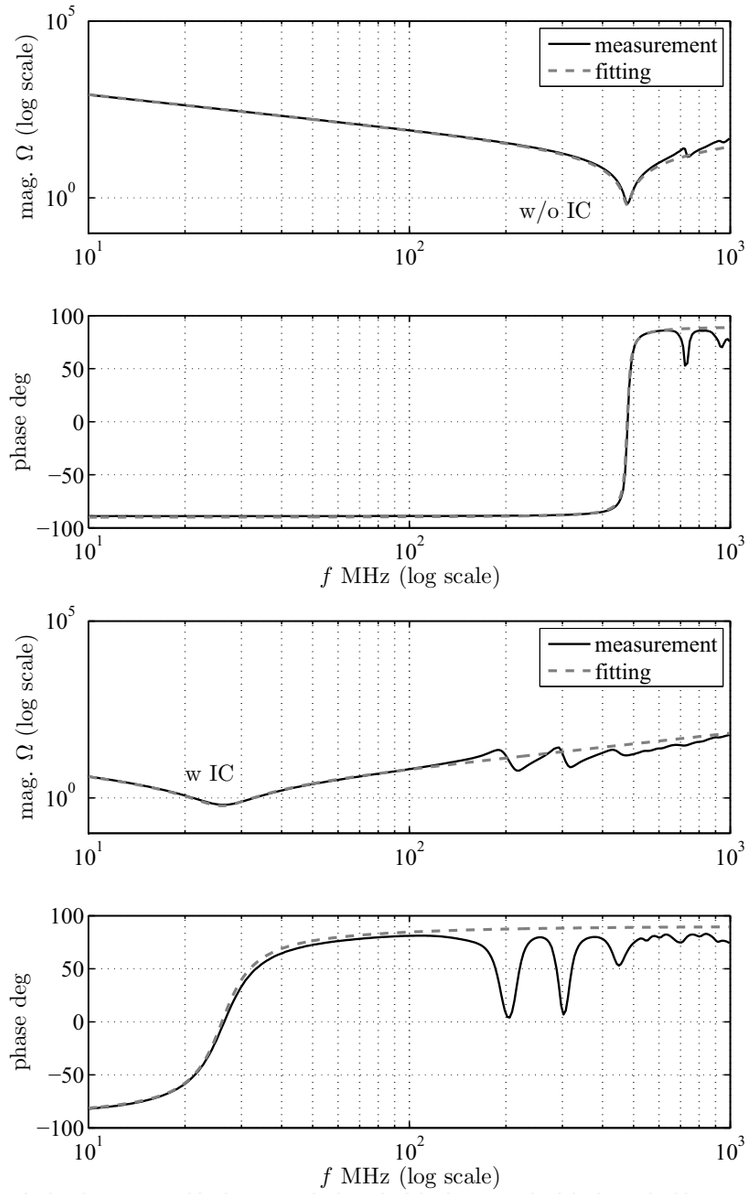
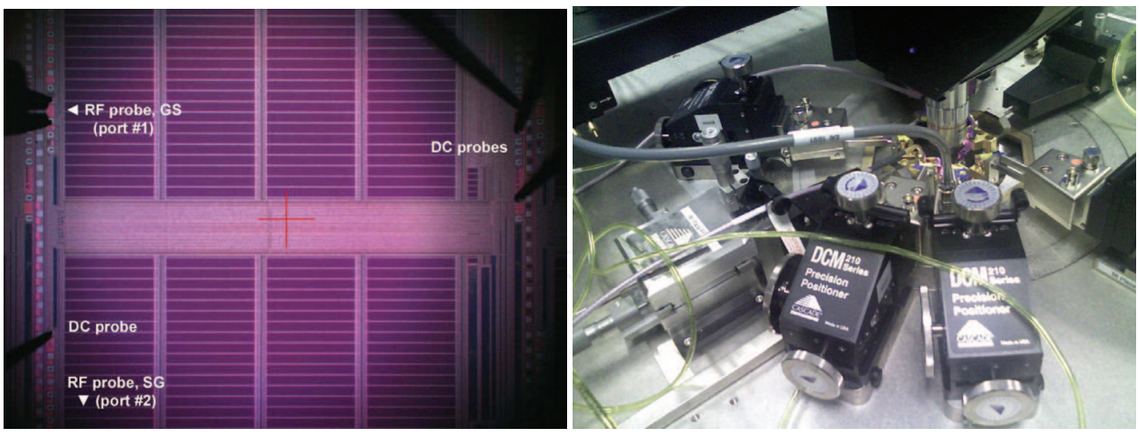


Fig. 7. Impedance seen from the terminals of the resistor of Fig. 4 without and with the IC mounted on it. Solid lines: real measurement carried out on the test board of Fig. 5; dashed lines: prediction obtained via the equivalent of Fig. 4 ($L = 5\,\text{nH}$, $L_b = 5.8\,\text{nH}$ $C_b = 19.15\,\text{pF}$ $r = 01.\,\Omega$, $R_b = 0.6\,\Omega$ and $Z_e(s) \approx 1/sC$, with $C = 3.45\,\text{nF}$.

Figure 9 confirms the dominant capacitive behavior of the core power network already observe in the curves of Fig. 7.

If needed, the accuracy of the fitting can be improved by considering the inherent multiport nature of the die and a two-pole equivalent (e.g., see (Stievano et al., 2011b) for additional details). Briefly speaking, this extension is achieved by considering a multiport Norton equivalent that replaces the model of Fig. 3*a* and a modified version of the test setup of Fig. 4.



(a) Memory die (b) RF and DC probes

Fig. 8. On-wafer measurement setup used for the estimation of the equivalent impedance of the core power delivery network.

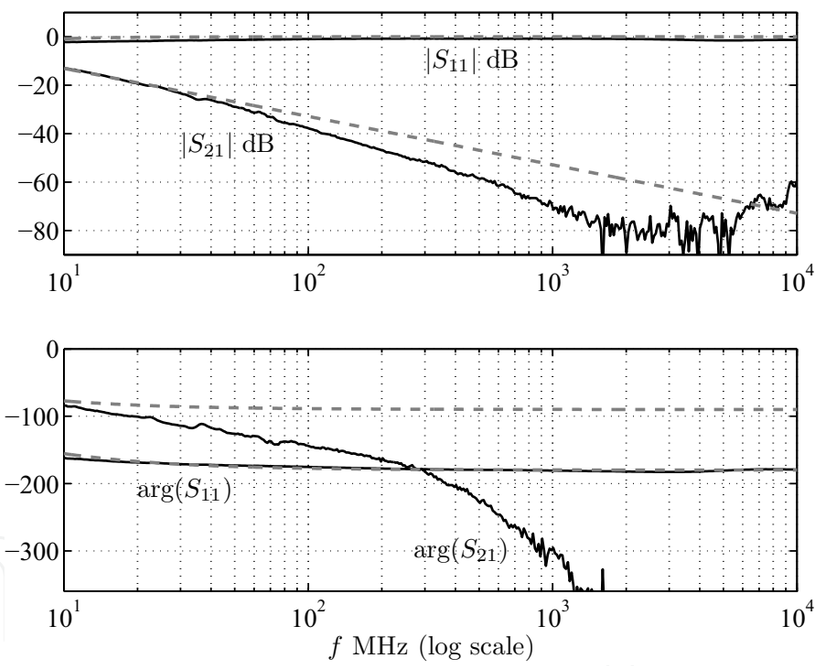


Fig. 9. Selection of the scattering responses of the VDD-VSS structure. Solid lines: reference measured responses; dashed lines: responses of lumped capacitor $Z_e(s) = 1/sC$.

4.2 I/O buffers

This section outlines the step-by-step modeling procedure for the generation of IC output port behavioral models. As discussed in Sec. 2.3, a behavioral model of an input port can be considered as a special case only (see (Stievano et al., 2004; 2011a) for additional details).
In order to devise a robust modeling procedure from real measurements carried out on a test board, the general two-piece model structure defined by (1) is particularized as follows.

$$\begin{cases} i(t) & = w_H(t)[i_{sH}(v_{dd}-v)+i_{dH}(v_{dd}-v,\frac{d}{dt}\ldots)]+ \\ & \quad w_L(t)[i_{sL}(v)+i_{dL}(v,d/dt)] \\ i_{dd}(t) & = w_H(t)i_{sH}(v_{dd}-v)+i_{dH}(v_{dd}-v,\frac{d}{dt}\ldots) \end{cases} \tag{3}$$

In the above equation, the output port current is a weighted combination of two submodels accounting for the buffer behavior in the fixed high and low logic states (i.e., $i_{H,L}$ of (1)) that are split into the sum of a static $i_{sH,L}$ and of a dynamic $i_{dH,L}$ contributions to facilitate model estimation and to make the modeling procedure more robust. Also, the specific choice of the variables in (3) as well as the model structure for the description of the power supply current have been adopted to facilitate the parameter estimation from measurements by incorporating in the model equations the typical operation of CMOS output buffers. Specifically, the main contribution of the power supply current i_{dd} of a CMOS buffer is the one drawn during the driver operation in the high output state and therefore provided by the corresponding contibution of the output port current model in the high state.

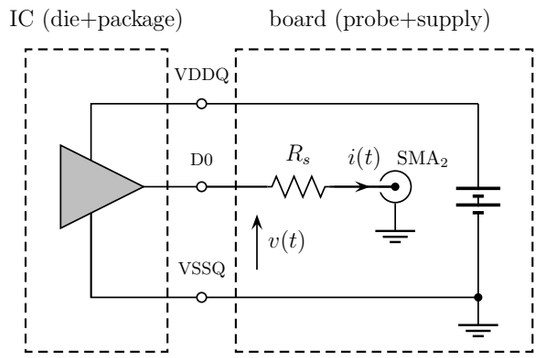


Fig. 10. Simplified equivalent of the setup used for the measurement of the port transient voltage and current of the I/O buffer of a digital IC. Current is indirectly measured through the voltage drop on the series resistor R_S (e.g., Rs=47 Ω).

Once the model structure (3) is assumed, the model parameters can be obtained via the following procedure that is based on the ideal setup shown in Fig. 10.

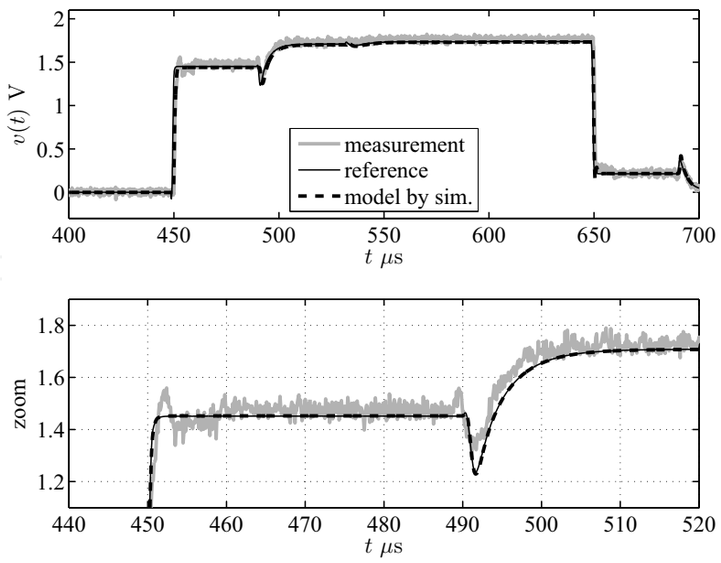
1. *Estimation of the buffer static characteristics.* In principle, the estimation of the device static characteristics $i_{sH,L}$ can be done by collecting a number of voltage-current pairs $\{v,i\}$ that are observed while an ideal voltage source is applied to the output port of the buffer and the source produces a DC sweep (this is also suggested by the IBIS specification (IBIS, 2008)). However, to simplify the modeling setup and to avoid dedicated test fixtures for the extraction of the static curves only, a different solution has been proposed: the buffer under modeling is driven to produce a periodic "01" bit pattern on a transmission line load that is plugged into the SMA$_2$ connector of Fig. 10. A transmission line load forces the port voltage and current waveforms to produce a stepped response. Hence, the static values of the buffer characteristics are extracted from the flat parts of the responses as described in (Stievano et. al., 2008; Stievano et al., 2011a).

   It is worth noticing that the number of static points used to approximate the static characteristics of the buffer is defined by the number of steps that are in general $3 \div 5$ for typical buffer circuits loading 50 Ω distributed interconnects. Also, no specific care must be paid in designing the distributed load. A simple 50 Ω coaxial cable or the shunt connection

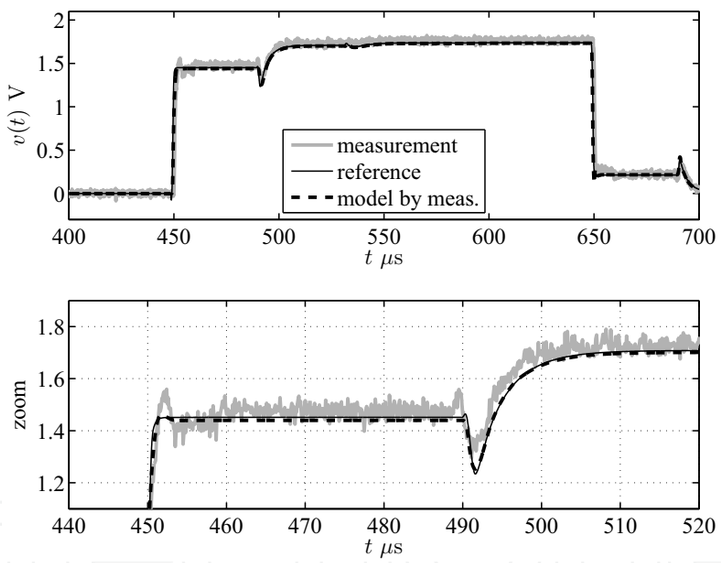
of two cables are sufficient to generate a set of responses with some steps. The only design parameter is the line length, that decides the timing of reflections and the duration of the flat responses, and that must be chosen on the basis of the device transition times. Roughly speaking, a device with 300 ps rise time would require a $1.5 \div 3$ m long transmission line.

2. *Estimation of the dynamical submodels.* The dynamical models used for i_{dH} and i_{dL} in (3) can be either defined by lumped circuit element (IBIS assumes a capacitor (IBIS, 2008)) or discrete-time parametric representations, whose parameters can be estimated by standard algorithms as in (Stievano et. al., 2008). For the latter case, the device responses used to feed the estimation algorithm are the slices of the voltage and current responses of the buffer on a distributed load recorded while the device is in the high (low) logic state.
3. *Computation of weighting coefficients.* The weighting signals w_H and w_L are computed after the estimation of the submodels $i_{sH,L}$ and $i_{dH,L}$ from the portion of the port responses occurring during state switching, as discussed in (Stievano et. al., 2008; Stievano et al., 2011a). In our problem, this amounts to solving the single linear equation (3) of the output current where v and i are the advocated voltage and current responses recorded during a single transition event and w_L is assumed to be $w_L = (1 - w_H)$. In principle, such an assumption can be removed and two sets of port responses can be used to compute two independent w_H and w_L signals. However, the latter simplification benefits the quality of the complete model since it reduces possible ill-conditioning or inaccuracies of the solution of the linear problem arising from noisy measured data or from the approximated responses of the static and the dynamic submodels in (3).
4. *Model implementation.* Finally, the last step of the modeling process amounts to translating the model equations in a simulation environment. This can be done by representing the equation (3) in terms of an equivalent circuit and then implementing such circuit as a SPICE-like subcircuit. The circuit interpretation of model equations is a standard procedure that is based on the use of controlled-current sources for the static contributions, and on resistors, capacitors, and controlled source elements for the dynamic parts (Stievano et al., 2004). As an alternative, model (3) can be directly plugged into a mixed-signal simulation environment by describing model equations via metalanguages like Verilog-AMS or VHDL-AMS. In this work, the obtained models have been implemented in SPICE.

It is worth noting that the ideal setup of Fig. 10 assumes that the series resistor R_S will be mounted as close as possible to the IC in order to neglect the possible effects of the board trace connecting the D0 ball to the SMD component.
The waveforms corresponding to the validation of the model for the D0 buffer of the example memory chip built in this way are shown in Fig. 11. The validation test consists of the the D0 buffer producing a periodic "01" switching on a 4m long RG58 coaxial cable plugged into the SMA_2 connector of Fig. 5 terminated by a 82 pF capacitor. Figure 11 collects the measured response, the reference response of the high-order transistor-level model of the buffer provided by the foundry and the responses of two models estimated from simulation (see the top panel (a)) and from measurements (see the bottom panel (b)). The very good agreement among the curves of Fig. 11 confirms the strengths of the proposed methodology in generating accurate models from measured and simulated responses. Such models can be easily obtained by the proposed procedure and can effectively replace the hardly available and less efficient transistor-level models of ICs.



(a) Model by simulation via the procedure in Stievano et al. (2004).



(b) Model by measurement.

Fig. 11. Port voltage responses of the D0 buffer for the validation tests considered in this study (see text for details). Top panel (a) compares measured responses with the reference responses of a transistor-level model and of a model generated from simulation; bottom panel (b) compares measured responses with the reference responses of a transistor-level model and of a model generated from measured data.

4.3 Power rail

The most suitable solution for the estimation of the lumped elements defining the model of the IC power rail structures (see Fig. 3*c*) is based on on-chip probing since the possible alternative on-board measurements are troublesome and would limit the possibility of

parameters estimation. The main reason is twofold: (i) the values of the *RLC* elements of the blocks of Fig. 3*c* are much lower than those of the corresponding parasitic elements of the package and test fixture and (ii) a custom package needs to be used since the VDDQ*n* and VSSQ*n* pads must be kept floating to avoid the undesired grounding effects of the bonding wires distributed along the rail. If the latter option is the only possible solution, a clever de-embedding strategy and parameters estimation procedure must be devised and adopted.
In this study, as already done for the core power delivery network, a VNA and two RF probes can be used to carry out the on-chip scattering responses of the power rail network. The probes are connected to the first and last pairs of VDDQ/VSSQ pads. Once the measurements are recorded, the parameters of the lumped models of Fig. 3*c* are obtained by least squares fitting. Figure 12 shows an example of the fitting, thus demonstrating the accuracy of the assumption of a model defined by the cascade connection of lumped blocks.
It is relevant to remark that the measurements carried out on the example memory chip include the mainly capacitive effects of the active devices, i.e., of the I/O buffers. Due to the typical large value of the buffers capacitance, the *C* value of the lumped *RLC* blocks of Fig. 3*c* can be hardly obtained from measurements and can be neglected.

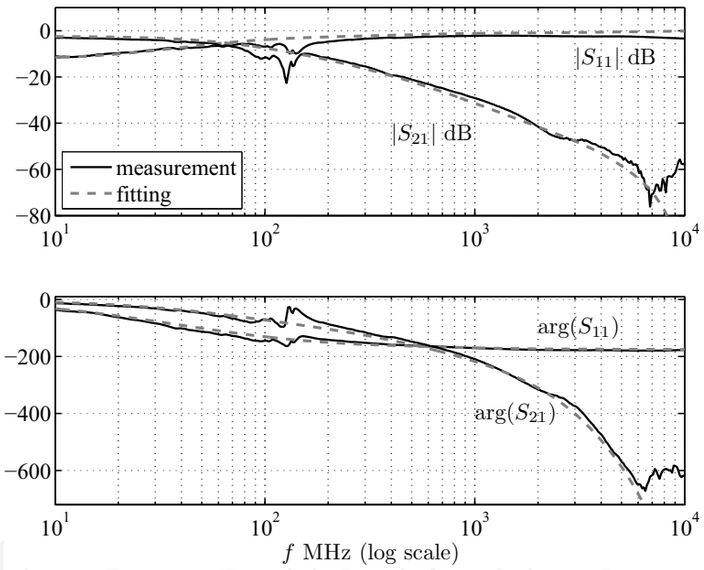


Fig. 12. Selection of the scattering responses of the power rail structure carried out between the first and the last pair of VDDQ-VSSQ pads, for the example test-case. Solid line: on-chip measurements; dashed line: responses by means of the simplified equivalent of Fig. 3*c*.

5. Conclusions

In this Chapter, the generation of a behavioral model of a memory IC is thoroughly discussed. Based on the physical structure of this class of devices, the proposed strategy amounts to defining three different classes of submodels for the description of the core and buffer power delivery network and of the I/O buffers of a memory device. State-of-the-art methodologies are used to generate models from both simulations and real measurements carried out on a board. Specific emphasis was given on model generation from real measured data with the aim of highlighting possible difficulties and inherent limitation in the generation of

the responses required by the modeling process. The feasibility of the modeling approach was demonstrated on a commercial IC Flash memory from measurements carried out on a specifically designed test board.

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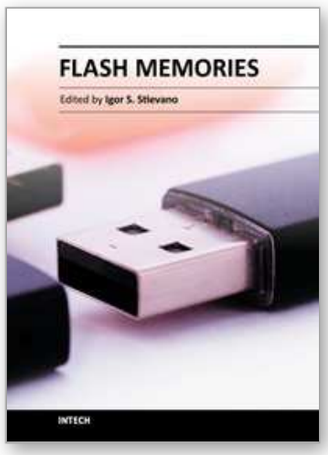

Flash Memories

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Flash memories and memory systems are key resources for the development of electronic products implementing converging technologies or exploiting solid-state memory disks. This book illustrates state-of-the-art technologies and research studies on Flash memories. Topics in modeling, design, programming, and materials for memories are covered along with real application examples.

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