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Performance Improvement of CMOS APS Pixels using Photodiode Peripheral Utilization Method

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1. Introduction

Charge-coupled device (CCD) technology had been leading the field of solid-state imaging for over two decades, in terms of production yield and performance until a relatively new image sensor technology called active pixel sensor (APS) (Fossum, 1993), using existing CMOS facilities and processes, emerged as a potential replacement in the early 1990s. While CMOS APS technology was originally considered inferior, continuous improvements in cost, power consumption (Cho et al., 2000), dynamic range (Gonzo et al., 2002), blooming threshold, readout scheme and speed (Krymsky et al., 1999), low supply voltage operation (Cho et al., 2000), large array size (Meynants, 2005), radiation hardness (Eid et al., 2001), and smartness have achieved performance equal to or better than CCD technology (Agranov et al., 2005; Krymsky et al., 2003).

Electro-optical performance of a photodiode (PD) type APS pixel is directly related to physical properties of photodiode diffusion layer. Doping concentration, junction depth, junction grading, biasing conditions, and physical shape of the photodiode diffusion layer determine the pixel full-well capacity, which is one of the main performance benchmarks of the PD-APS pixel. Pixel full-well capacity is related to sensitivity, charge capacity, charge saturation, dynamic range, noise performance, and the spectral response of the pixel (Theuwissen, 1995). Pixel dynamic range versus full well capacity for different pixel noise levels could be plotted as shown on Fig. 1. Thus, increasing full well capacity is desirable.

In this chapter, so called photodiode peripheral utilization method (PPUM) is introduced addressing performance improvement of photodiode type CMOS APS pixels, (Ay, 2008). PPUM addresses the improvement of the metrics full well capacity and spectral response especially in blue spectrum (short wavelength). First, identification of junction and circuit parasitics and their use in improving the full-well capacity of a three-transistor (3T) PD-APS pixel through photodiode peripheral capacitance utilization is discussed. Next, spectral response improvement of PD-APS pixels by utilizing the lateral collection efficiency of the photodiode junction through PPUM is discussed. The PPUM method and its proposed benefits were proven on silicon by designing a multiple-test-pixel imager in a 0.5 μ m, 5V, 2P3M CMOS process. Measurement results and discussions are presented at the end of the chapter.

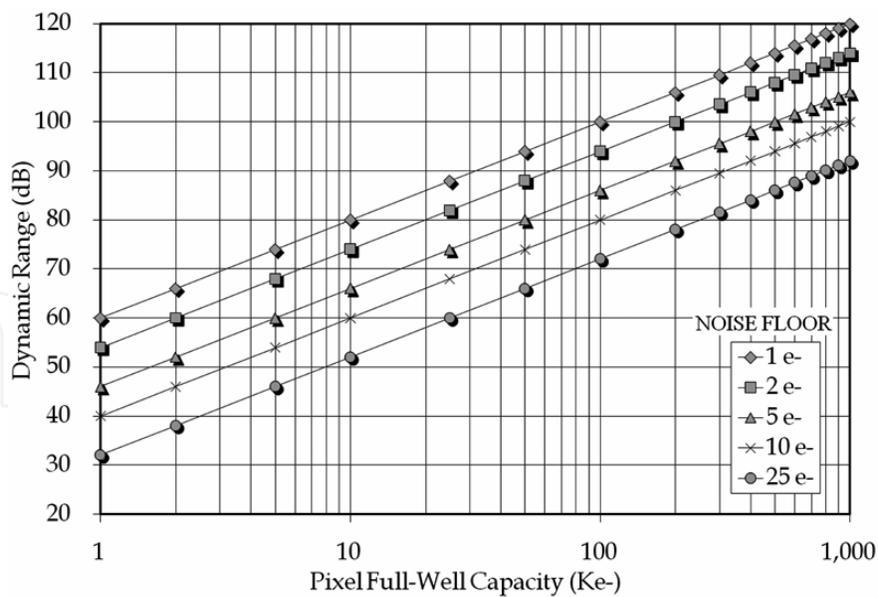


Fig. 1. Pixel dynamic range versus full well capacity and noise floor.

2. Photodiode Peripheral Utilization Method (PPUM)

The theory behind the photodiode peripheral utilization method (PPUM) is that, if the pixel pitch is restricted to a certain size, then pixel full-well capacity could be increased by opening holes in the photodiode's diffusion. These diffusion holes could be used to increase photodiode parasitic capacitance, by increasing the perimeter capacitance of the photodiode for certain process technologies shown on Fig 2. Diffusion holes also can increase spectral response of a photodiode by utilizing lateral collection of charges converted close to the semiconductor surface at the edges of photodiode, (Fossum, 1999; Lee and Hornsey, 2001).

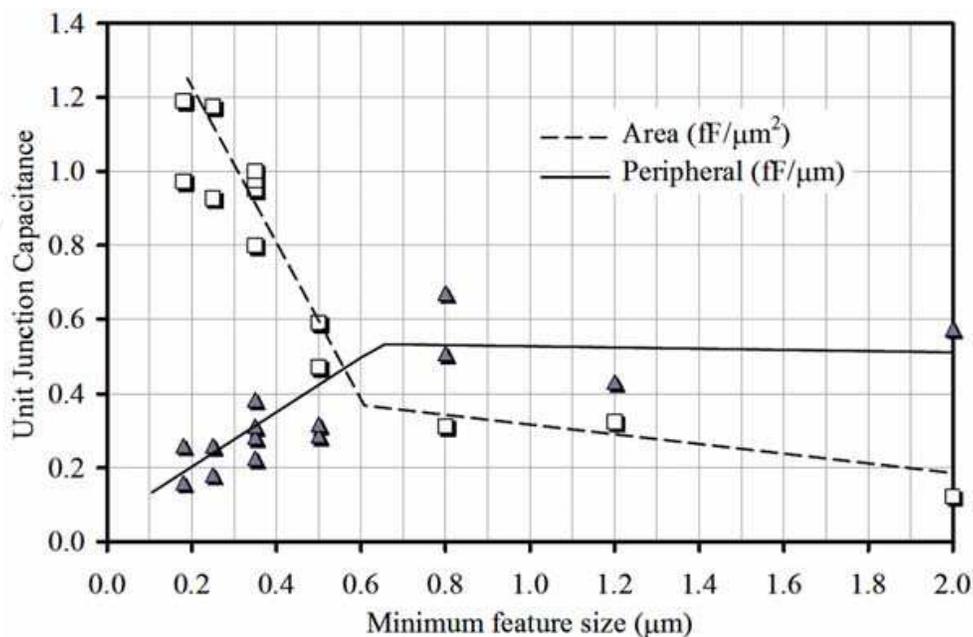


Fig. 2. Unit junction capacitance of CMOS processes, (Ay, 2004).

A reverse-biased PN-junction diode is used in photodiode (PD) type CMOS APS pixels as a photon conversion and charge (electron) storage element. The total capacitance of the photodiode diffusion layer determines key pixel performance parameters. For example, wide-dynamic-range pixels require large pixel full-well capacity and low readout noise. Photodiode full-well capacity is comprised of two components: bottom plate (area) and side wall (peripheral) junction parasitic capacitance. Designer controls the size of the photodiode diffusion bottom plate, while peripheral junction depth and doping concentration are process and technology dependent. The photodiode's unit area junction capacitance (C_A) and unit peripheral junction capacitance (C_P) are given in the following equations, (Theuwissen 1995), including technology and design parameters, for the first-order capacitance that contributes to total well capacity.

$$C_{PD} = C_A \cdot A + C_P \cdot P \quad (1)$$

$$C_{PD} = \frac{C_{J0A} \cdot A}{\left[1 - \frac{V_{PD}}{\Phi_B}\right]^{M_J}} + \frac{C_{J0SW} \cdot P}{\left[1 - \frac{V_{PD}}{\Phi_{BSW}}\right]^{M_{JSW}}} \quad (2)$$

where

C_A, C_P unit area junction capacitance and unit peripheral junction capacitances, respectively;

C_{J0A}, C_{J0SW} unit zero-bias area and peripheral junction capacitances, respectively;

A, P area and peripheral of the photodiode regions, respectively;

Φ_B, Φ_{BSW} built-in potential of area and side-wall junctions, respectively;

M_J, M_{JSW} junction grading coefficients of area and side-wall junctions, respectively;

V_{PD} photodiode junction voltage.

Other parasitic capacitances due to the reset and readout transistors in pixel contributing to total photodiode junction capacitance are shown in Fig. 3. for a three-transistor (3T) PD-APS pixel. These parasitic capacitances contribute to total pixel capacitance differently in different modes of pixel operation, (Ay, 2004). Right after photodiode reset and during scene integration periods, overlap capacitances C_{O1} and C_{O2} and gate-to-body capacitance of the

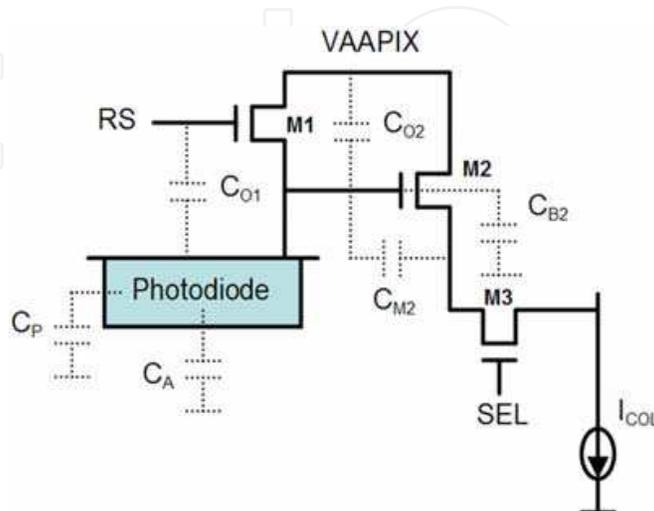


Fig. 3. Parasitic capacitances of photodiode type CMOS APS pixel.

readout transistor M2 (C_{B2}) add to the total photodiode capacitance. During a readout period, miller capacitance C_{M2} and overlap capacitances C_{O1} and C_{O2} contribute to the total photodiode capacitance. Contribution of pixel circuit parasitic capacitances is described by the following equations during imaging (3) and readout (4):

$$C_{\text{par,imaging}} = \left[W_{M1} \cdot L_{OL,M1} + W_{M2} \cdot \left[L_{M2} - L_{OL,M2} \right] \right] \cdot C_{OX} \quad (3)$$

$$C_{\text{par,read}} = \left[\frac{2}{3} \cdot W_{M2} \cdot \left[L_{M2} - 2 \cdot L_{OL,M2} \right] \cdot \left[1 - G \right] \right] \cdot C_{OX} \quad (4)$$

$$+ \left[W_{M1} \cdot L_{OL,M1} + W_{M2} \cdot L_{OL,M2} \cdot \left[2 - G \right] \right] \cdot C_{OX}$$

where

W_1, W_2 channel width of the reset and source-follower transistors, respectively;
 L_{OL1}, L_{OL2} channel overlap length of the reset and source-follower transistors, respectively;
 C_{OX} unit oxide capacitance,
 G pixel source follower gain factor.

C_A and C_P of a few CMOS process technologies, with minimum feature sizes $2.0\mu\text{m}$ – $0.18\mu\text{m}$, is shown in Fig. 2., (Ay, 2004). Unit-area capacitance is larger for deep sub-micron devices with a minimum feature size $<0.5\mu\text{m}$, due to the increased channel-stop doping-level (for better device isolation, higher diffusion doping concentrations, and shallower junction depths) (Packan, 2000). Thus, peripheral junction capacitance could be better utilized in processes that have equal or more unit peripheral junction capacitances than in processes with $<0.5\mu\text{m}$ feature sizes, by opening holes in the photodiode region. As will be shown in the next sections, this will not only improves the total full-well capacity of the pixel, but also improves the spectral response for detecting short wavelength photons.

3. Photodiode lateral collection improvement

The photosensitive element in APS pixels, the photodiode (PD), works in charge integration-mode where pixels are accessed at the end of a time interval called the integration period. When it is accessed, photodiode is read and then cleared for next scene integration. Fig. 4. shows the cross-section of a PN-junction photodiode formed in a CMOS process; the photodiode is reverse-biased and formed by using the shallow N+ doped, drain-source diffusion of an NMOS device. A bias voltage applied to the N+ region forms a depletion region around the metallurgical PN-junction, which is free of any charge because of the electrical field. Any electron-hole pairs generated in this region see the electrical field as shown in the AA' cross-section view of the photodiode in Fig.4. Electrons move in the opposite direction of the electric field (toward the N+ region), while holes move toward the P-region. As a result, electrons are collected in a charge pocket in the N+ region, while holes are recombined in the substrate. This type of photodiodes has been widely used in CMOS and early CCD-type image sensors as a photo conversion and collection element.

There are two issues associated with using the N+ drain/source diffusion of an NMOS transistor as photosensitive element. First is the dark current induced by stress centres around the diffusion, (Theuwissen 1995). These stress centres are formed during the field

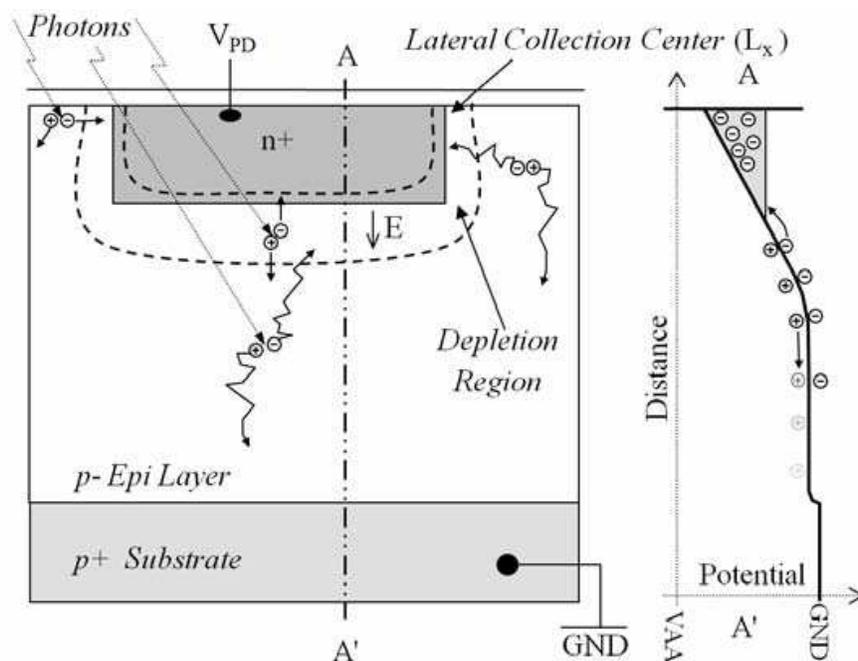


Fig. 4. a)Cross-section and b)potential-well diagram of a PN-photodiode.

oxide (FOX) formation in standard CMOS processes. The second issue is the surface-related dark current generated from the work function difference between the N+ diffusion surface and overlying isolation oxide layer. This second one causes surface recombination centers and defects. Both of them absorb photo-generated electron-hole pairs close to the surface, resulting in quantum loss at shorter wavelengths. As a result, silicon photodiodes show less sensitivity in the blue spectrum (<400nm. Most blue photons are collected through lateral diffusion of the carriers generated on or in the vicinity of a photodiode peripheral – known as peripheral photoresponse or lateral photocurrent (Lee et al., 2003). Thus, increasing lateral collection centers or peripheral length of a photodiode potentially improves collection efficiency for short-wavelength photons (Fossum, 1999; Lee et al., 2001) as it is depicted in Fig. 5. This method was adopted for UV photodiode devices in P-well CMOS processes (Ghazi et al.,2000).

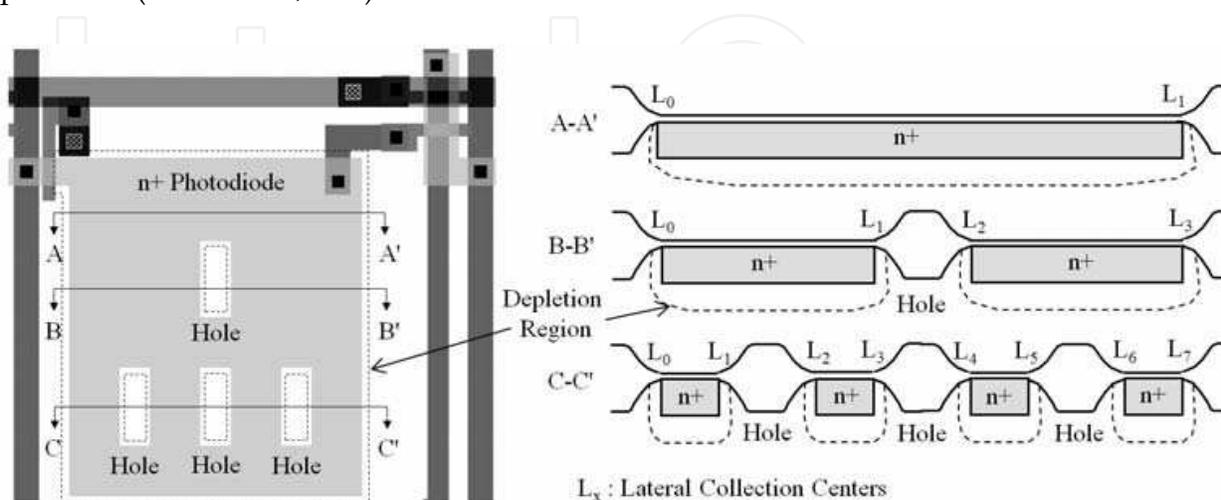


Fig. 5. Improving lateral collection by increasing photodiode peripheral for blue photons.

4. CMOS pixel design using PPUM

There are many ways to test CMOS imaging pixels using test vehicles. Some uses product grade imager platforms to test not only the performance of the imaging pixels, but also their performance in final product environment. Some uses very small array of dumb pixels to measure basic characteristics of the pixel under investigation. A commonly used architecture is called fully flexible open architecture (FFOA) that composes of sample and hold circuits, correlated double sampling (CDS) and differential delta sampling (DDS) circuits, and source follower amplifiers (Nixon et al, 1996; Mendis et al., 1997). Simple FFOA architecture gives very reliable and predictable signal path characteristics. It also allows multiple pixel types with different sizes to be integrated on the same chip.

A test imager was designed containing reference and pixels utilizing PPUM as proof of concept. The reference or baseline three-transistor (3T) photodiode type (PD) APS reference pixel (REF) is shown in Fig. 6. It was designed to normalize measurement results of the test pixels with diffusion holes. A fairly large pixel size of $18\mu\text{m} \times 18\mu\text{m}$ was chosen. It has circular-looking photodiode diffusion region for reducing overall dark current. Row select and reset signals were drawn on top of each other using horizontal metal-2 and metal-3 lines, and metal-1 was used on the vertical direction for routing pixel output and supply signals.

The reference photodiode diffusion area and peripheral were $141.7\mu\text{m}^2$ and $44.6\mu\text{m}$, respectively. Unit area and peripheral capacitance of the photodiode's N+ diffusion layer in used process were $0.25\text{fF}/\mu\text{m}^2$ and $0.22\text{fF}/\mu\text{m}$, respectively. Total pixel capacitance was calculated by including the Miller contribution of the source-follower transistor (M2) and other parasitic capacitances from equations (3) and (4). Miller contribution to the total photodiode capacitance at 0.75 source-follower gain was calculated to be 1.1fF ; peripheral junction capacitance made up of 20 percent of the total photodiode capacitance, and the total calculated photodiode capacitance was about 47.5fF .

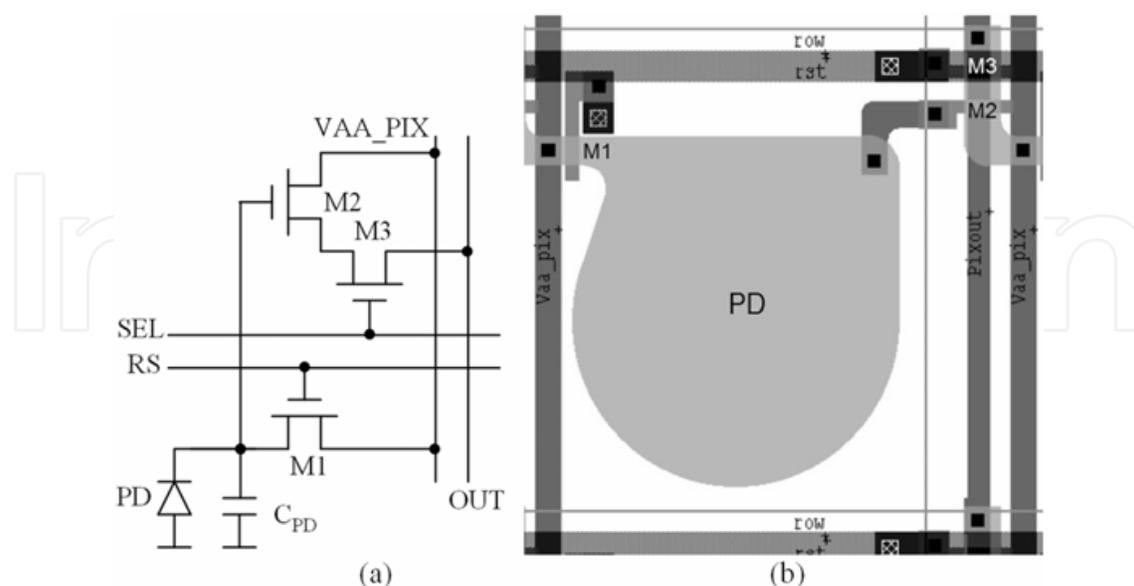


Fig. 6. 3T CMOS APS reference pixel (REF) a) schematic, b) layout.

Four test pixels with a number of circular diffusion openings were designed to model the peripheral utilization effect on pixel performance, with layouts shown in Fig. 7. Pixels have

1.6 μm -diameter circular holes on the photodiode diffusion with the same base as the reference pixel (REF). The total number of circular diffusion holes was 17, 14, 11, and 7 for pixel layouts called c17, c14, c11, and c7, respectively. Holes were randomly placed on the reference design. Again, the circular shape was chosen for holes to reduce stress-related dark current.

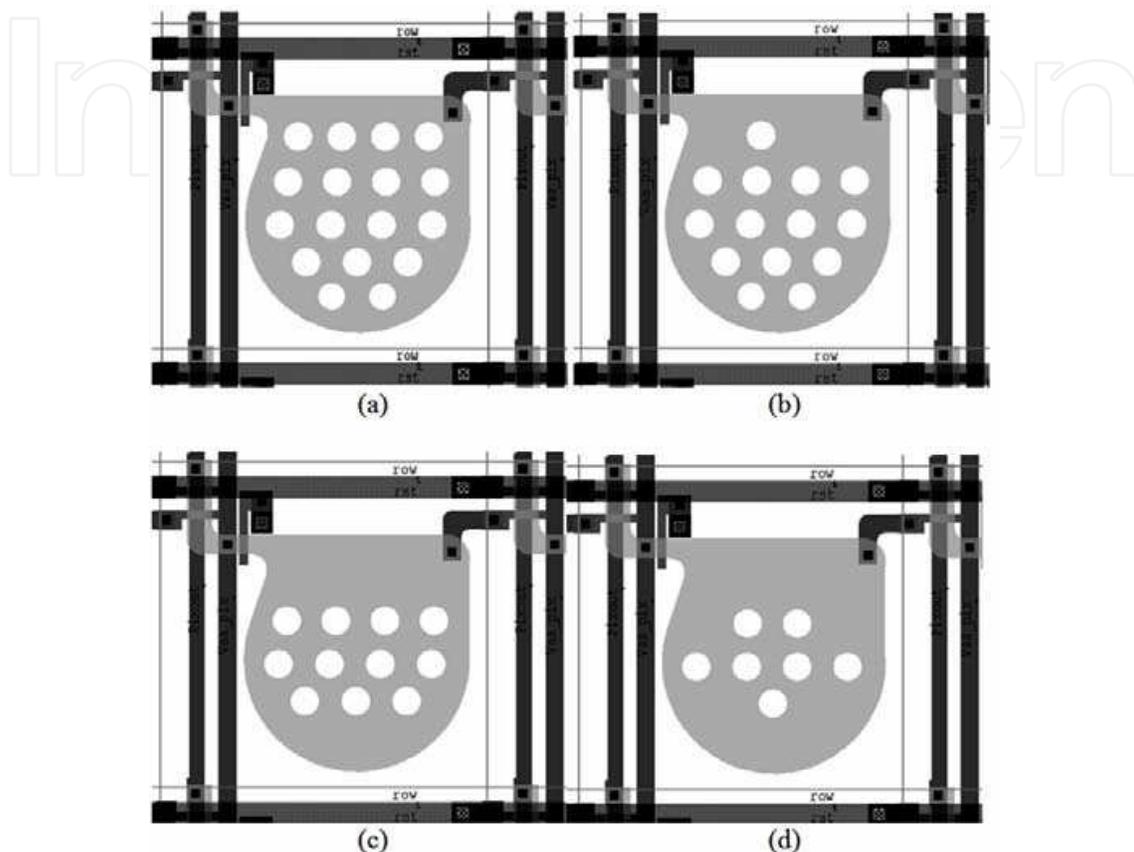


Fig. 7. Test pixels with circular openings; a) c17, b) c14, c) c11, d) c7

5. CMOS APS imager design

All test pixels were placed in the same imager to compare performance under common imaging and environmental conditions. Single-channel serial-readout architecture was adopted to pass all pixel signals through the same signal path for accurate comparison of the effects (Ay et al., 2002). Imagers were composed of a 424x424 pixel array, row decoder and drivers, timing generators, digital and analog buffers, a column analog signal processor (ASP), a column decoder and multiplexer, and a single, global readout channel. The pixel array was divided into 16 different subsections with 106 x 106 pixel arrays, with different pixel designs in each subsection. A shift-register type decoder was used in the column, too. Decoder control signals were generated in the timing generator block separately for frame operation. A pseudo-differential charge amplifier and sample-and-hold circuits were used in the global readout block. Chip outputs were in differential analog signals (SIG) and reset (RST). Signal analog-to-digital conversion used an analog-frame-grabber card.

A detailed schematic of the prototype imager's analog signal chain is shown in Fig. 8. Each column contains a PMOS source follower, two sample-and-hold capacitors and a number of

switches. A PMOS source follower was used for level shifting and signal amplification. Column signals were read during column time through single channel, pseudo-differential charge amplifiers and buffered for off-chip analog-to-digital conversion.

Fig. 9. shows a microphotograph of the prototype imager. The prototype was designed in 0.5 μm , 5V, 2P3M CMOS process, and different test pixel quadrants could be recognized on the pixel array with the naked eye. Table 1 provides specifications for the prototype imager. Global charge amplifier gain was adjusted so that the gain-loss in pixel and column source followers balanced to achieve unity gain from pixel-to-chip output. Operating at 5 Mp/s readout speed, the prototype achieved a 30-frame per second (FPS) frame rate. A 5V supply was used and the total power consumption of the chip was <200mW. Noise floor of the readout channel was 850 μV .

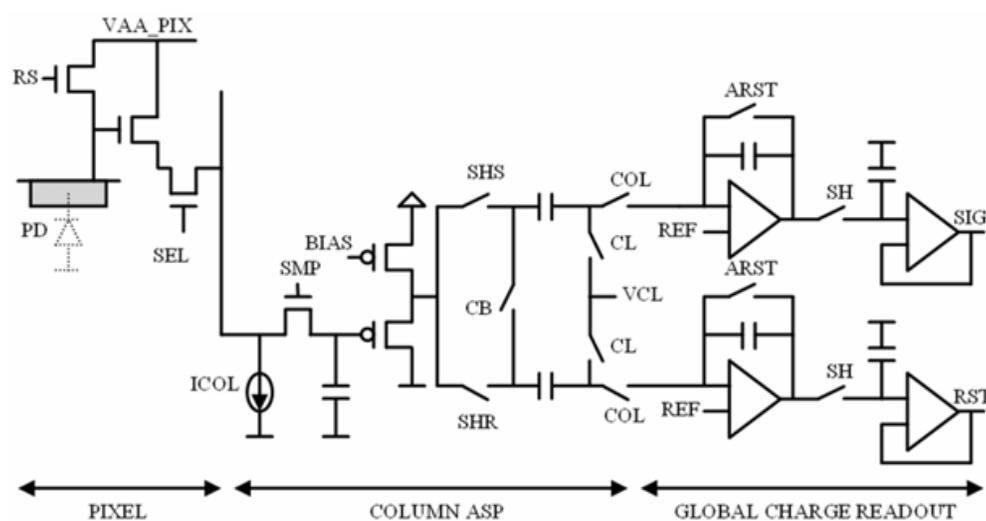


Fig. 8. Analog signal chain from pixel to chip output.

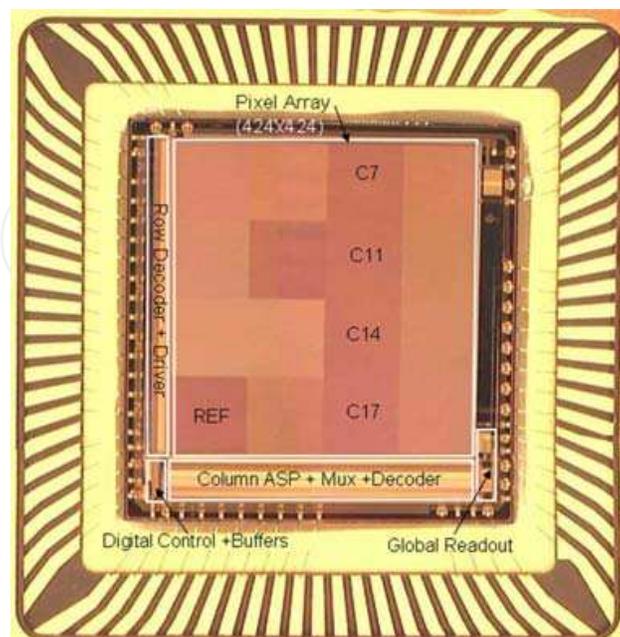


Fig. 9. Micrograph of Prototype CMOS APS imager chip.

Array Size	424 x 424
Pixel Size	18 μm x 18 μm
Pixel Type	3T Photodiode APS
Technology	0.5 μm CMOS (2P3M)
Output Format	Differential Analog
Frame Rate	30 FPS
Gain (photodiode to chip output)	1.0 V/V
Noise Floor	850 μVolt
Fixed Pattern Noise (FPN)	< 0.25 (% Vsat)
Power Supply (VAA,VAA_PIX)	5 Volt
Power Consumption	< 200 mWatts
Package	PGA 84L
Chip Size	9.75 mm x 9.75 mm

Table 1. Design specifications of the prototype CMOS imager

6. Measurement results

Electrical and optical characteristics of reference and circular-opening test pixels measured under the same environmental and imaging conditions, (Ay, 2004). Having them integrated on same focal plane array make these measurements more manageable and easy.

6.1 Reference pixel measurements

Dark current was measured at room temperature. It was 10.63 mVolt per second. This equals to 3155 e-/sec with the measured conversion gain of 3.37 μVolt per electrons. Measured photon transfer curve of the reference pixel is shown in Fig. 10. Total measured pixel capacitance was 47.5 fF as oppose to the calculated value of 46.5fF. Measured pixel full-well capacity was 508Ke- with 1.714V effective photodiode voltage.

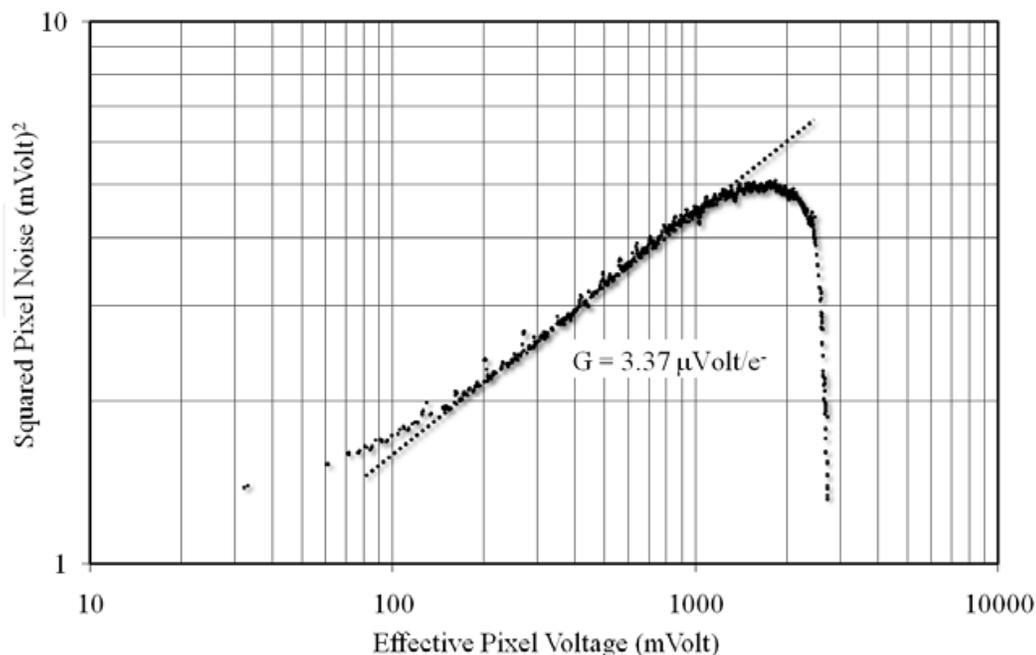


Fig. 10. Measured photon transfer curve of the reference pixel (REF1).

Measured light sensitivity was 2.44 Volt/Lux*sec while peak quantum efficiency was 48.55 percent at 500nm as shown in Fig.11. At 400nm, quantum efficiency of the reference pixel was 23.4 percent. Dynamic range of the reference pixel was around 66.4 dB because of the higher noise floor measured. Rest of the measurement and calculations are listed in Table 2 for the reference pixel (REF1). All measurements of the test pixels with diffusion holes are normalized with the reference pixel characteristics.

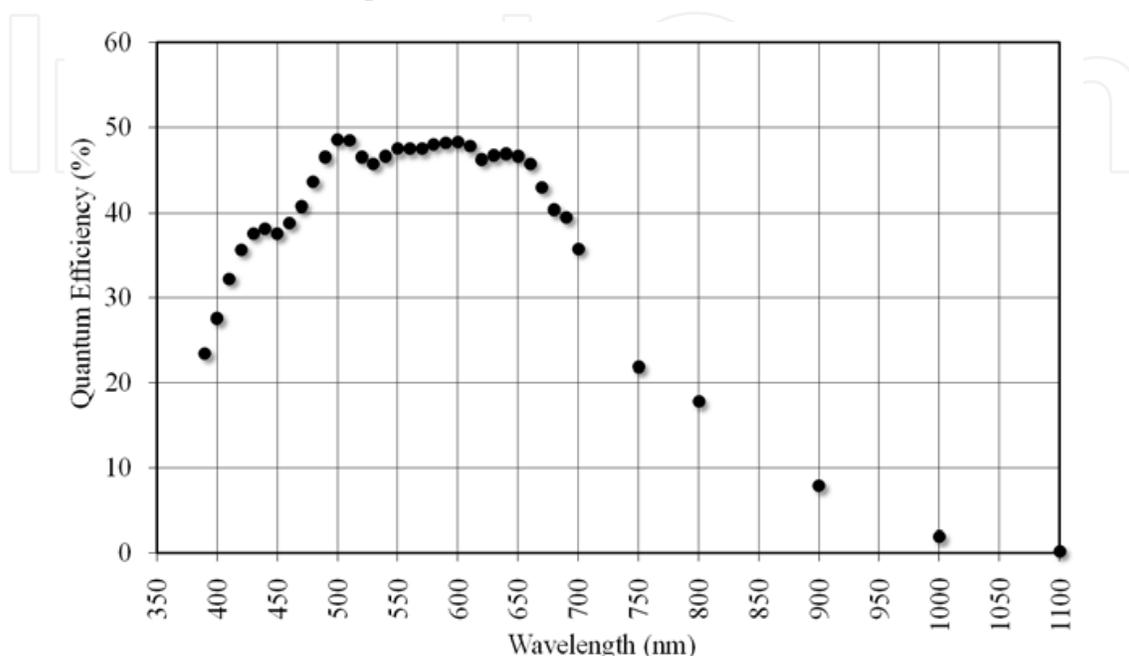


Fig. 11. Measured quantum efficiency of the reference pixel (REF1).

Parameter	Measured	Calculated	Unit
Sensitivity	2.44		Volt/lux.sec
Light Saturation	1.07		lux.sec
Saturation Voltage	2.74		Volt
Quantum Efficiency	23.41		at 390nm
	47.44		at 550nm
	48.55		peak
Conversion Gain	3.370	3.446	$\mu\text{V}/\text{e}^-$
Full Well	1.714	1.714	Volt
	508,736	497,530	e^-
Pixel Capacitance	47.54	46.49	fF
Dark Current	10.63		mVolt/sec
	3155		e^-/sec
Dynamic Range	66.39	79.67	dB

Table 2. Calculated and measured parameters of the reference pixel (REF1).

6.2 Conversion gain and pixel full-well capacity measurements

Conversion gain and the full-well saturation voltage of the reference and test pixels were measured to determine pixel well capacity. Measurement results are shown in Fig. 12. Pixel

well capacity increases with proper utilization of the photodiode peripheral junction, by using the holes on the photodiode diffusion region. Conversion gain of the pixel reduces with increased pixel capacitance, and the pixel full-well capacity increases.

It was observed that a linear correlation between total peripheral capacitance and pixel full-well capacity exist, because C_A is almost equal to C_P in the process used. The area loss was compensated for by the peripheral increase, by a factor of 2.5. Because the radius of the opening was set to $0.8\mu\text{m}$, and the opening peripheral was ($p = 2\pi r$) $5.027\mu\text{m}$ while the area was ($a = \pi r^2$) $2.01\mu\text{m}^2$. A factor of four could easily be achieved by choosing an opening radius of approximately $0.5\mu\text{m}$. However, reducing diameter results in depletion region overlap, and lowers peripheral capacitance and utilization.

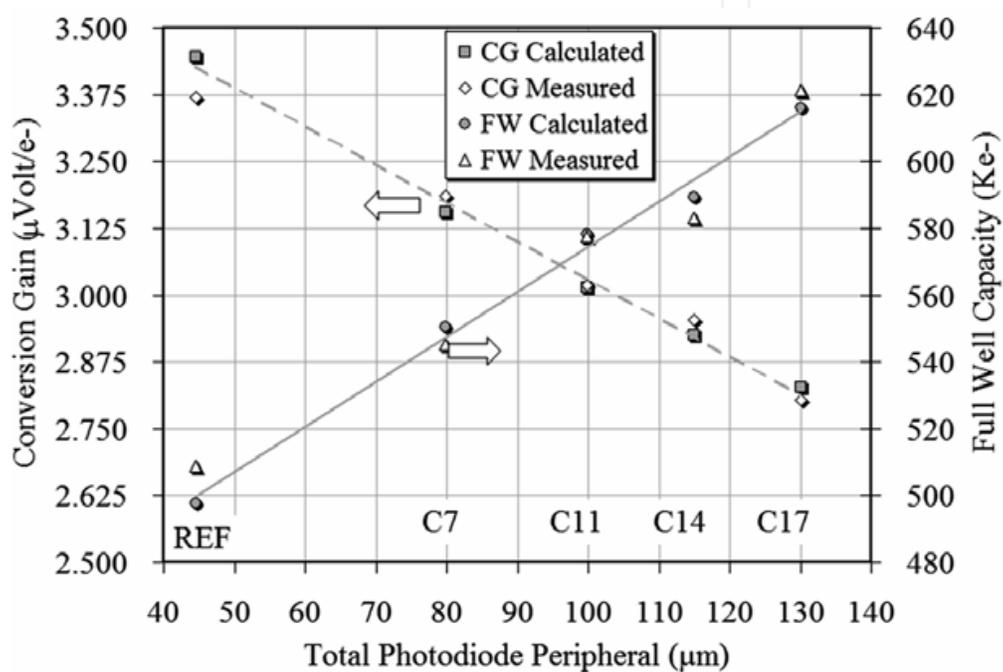


Fig. 12. Conversion gain and full-well capacity of the pixels.

6.3 Quantum Efficiencies (QE)

Quantum efficiencies (QE) of the reference (REF) and test pixels were measured by using a very stable light source, a monochromator, and a calibrated photodiode. Measurement was performed between 390nm and 700nm , with 10nm steps. QE measurement results for reference (REF) and test pixels (c17, c14, c11) are shown in Fig. 13. In the figure, QE difference between the reference pixel and a test pixel with 17 openings (c17), normalized by reference QE, was also plotted. Spectral response improvement was observed with an increased number of openings on the photodiode. The most improvement was achieved at the shorter wavelengths and large number of openings, which is more visible in Fig. 14.

Blue photons generated as electron-hole pairs close to the surface of the silicon were collected better laterally at close surroundings of the photodiode area. By adding circular openings these lateral collection areas were increased, which leads to a better QE response at shorter wavelengths. However, deep-penetrating photon collection probability did not increase as much as that of surface photons, giving less improvement in longer wavelengths.

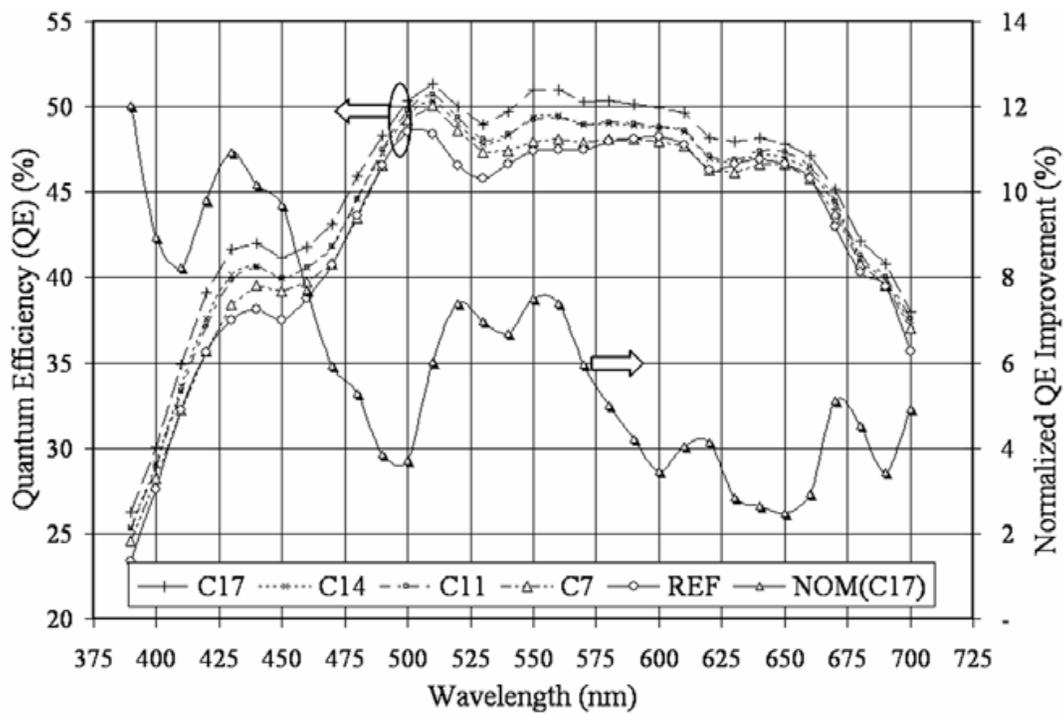


Fig. 13. Quantum efficiency of the test and reference pixels.

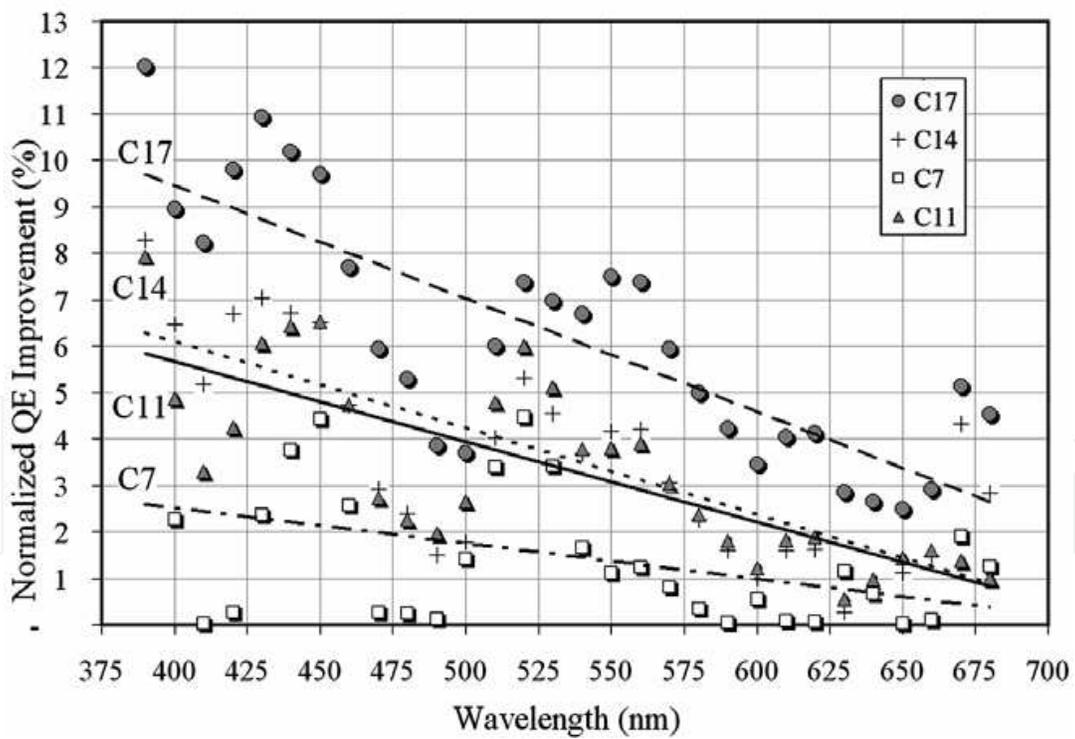


Fig. 14. Quantum efficiency improvement trends of test pixels.

6.4. Dark current

Measured dark current for the reference pixel was 10.63 mV/s at room temperature, or 3155 e-/s with the measured conversion gain of 3.37μV per electron. More dark current was

observed from the test pixels with longer peripherals than the reference pixel, as shown in Fig. 15. Dark current, in terms of electrons per second, increases by approximately one-third of the reference dark electrons when the photodiode peripheral doubles (assuming the surface dark current effect was neglected).

In reality, measured dark current has two components, surface dark current and stress-center-related dark current. Surface dark current is related to the area of the photodiode, while stress-center-based dark current is related to the peripheral region. Opening a hole on a photodiode region reduces the surface contribution and increases the peripheral contribution on the total dark current. It is possible to determine the contribution of these two components of the dark current by designing fixed-area and varying-peripheral test pixels.

Dark current also increases noise floor effectively working against the gain achieved by PPMU method. In current design this contribution was not observed because the readout noise was larger than the dark current shot noise in low light condition. Measured dynamic range was around 66dB due to the higher readout channel noise. Dark current electrons add up on pixel capacity, yet, their contribution is less than 0.5% of the full well in worst case.

6.5 Sensitivity

Sensitivity of the test and reference pixels were measured with a very sharp green (550nm \pm 20nm) bandpass filter at 175ms integration time. Measurement results are shown in Figure 13. Sensitivity's correlation with pixel capacity was extracted by fixing the light wavelength, pixel fill factor, and integration time. It was observed that the higher the pixel capacity, the lower the sensitivity was, for an inverse correlation. A 20 percent increase in pixel capacity causes a 17 percent decrease in pixel sensitivity between reference and test pixels with 17 openings, as shown in Fig. 16.

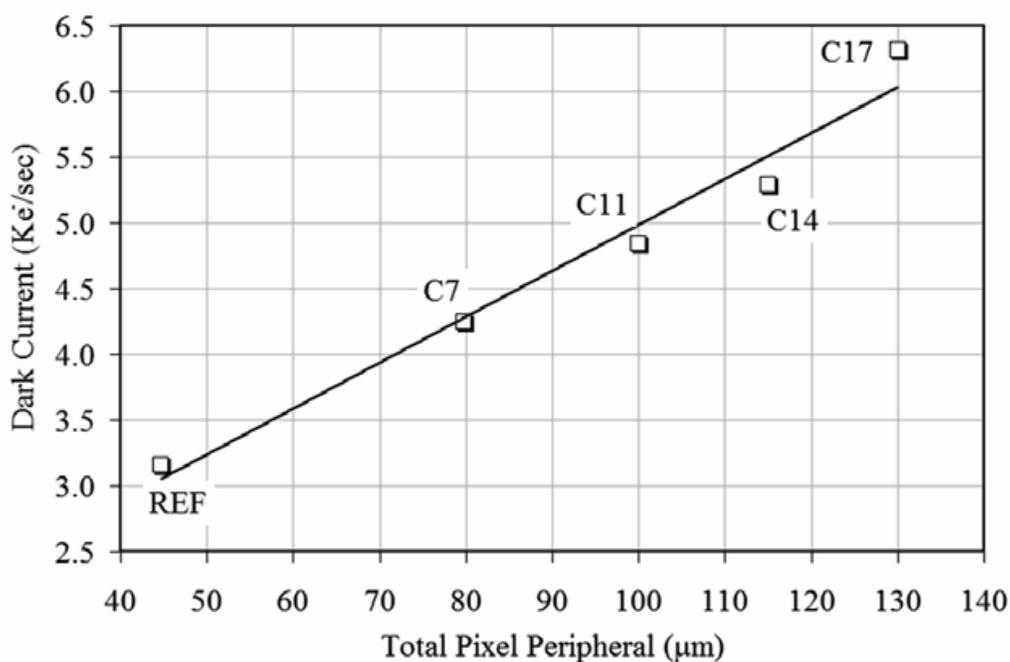


Fig. 15. Measured dark current rates of reference and test pixels.

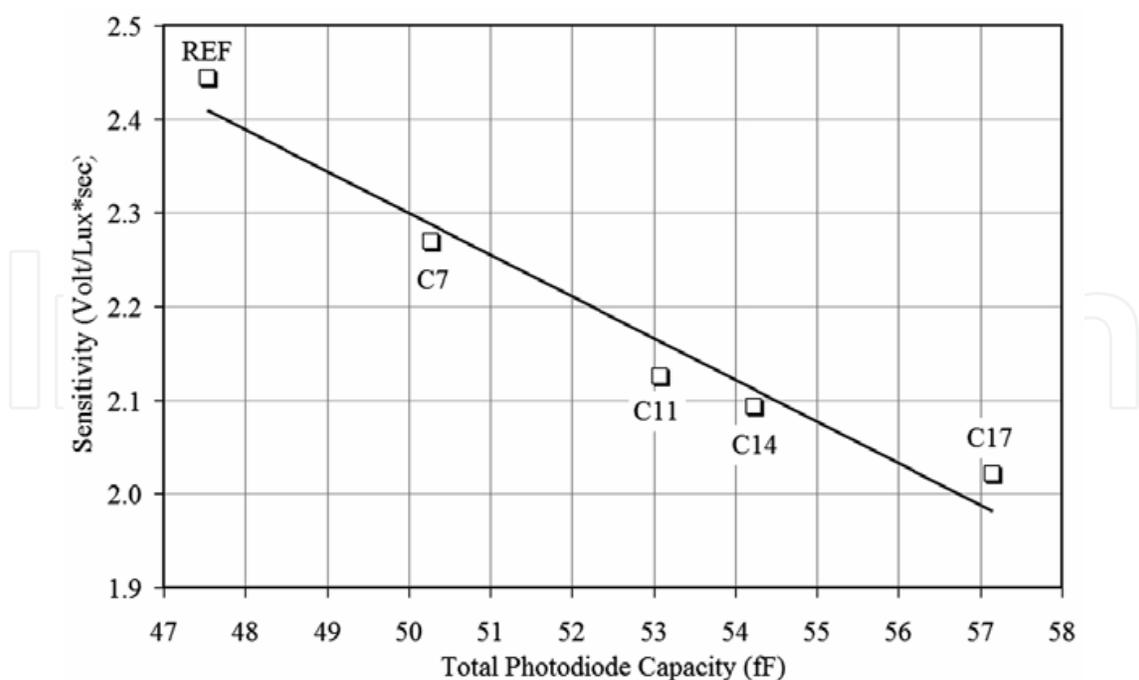


Fig. 16. Measured sensitivity of the reference and test pixels.

7. Conclusion

Photodiode-type CMOS APS pixels' quantum efficiency was improved by opening number of circular holes on the photodiode diffusion area of a prototype imager. A method called photodiode peripheral utilization method (PPUM) was developed to accommodate pixel performance improvement in a fixed size pixel. Utilizing PPUM, four test pixels with 7, 11, 14, and 17 circular openings, and a reference pixel (REF), were designed, fabricated, and tested in a prototype APS imager made with a 0.5 μm , 5V, 2P3M CMOS process. Measured pixel characteristics are summarized in Table 3.

Pixel Design	C17	C14	C11	C7	REF	Unit
PD Area	107.5	113.5	119.6	127.6	141.7	μm^2
PD Peripheral	130.1	115.0	99.9	79.8	44.6	μm
Dark Current	6.31	5.29	4.84	4.25	3.15	Ke-/sec.
Conversion Gain	2.80	2.95	3.02	3.19	3.37	$\mu\text{Volt}/e^-$
Quantum Efficiency	26.22	25.34	25.26	24.58	23.41	% @ 390nm
	51.00	49.41	49.24	47.97	47.44	% @ 550nm
	51.31	50.35	50.72	50.05	48.55	% @ peak
QE improvement	12.0	8.3	7.9	5.0	0.0	%QE _{REF} @390nm
	7.5	4.2	3.8	1.1	0.0	%QE _{REF} @550nm
Sensitivity	2.02	2.09	2.13	2.27	2.44	Volt/Lux.sec
Pixel Full-Well Depth	621.4	583.1	577.6	545.2	508.7	Ke-
Pixel Full-Well Improvement	22.1	14.6	13.5	7.2	0.0	%FW _{REF}
Pixel Capacitance	57.1	54.2	53.1	50.3	47.5	fF

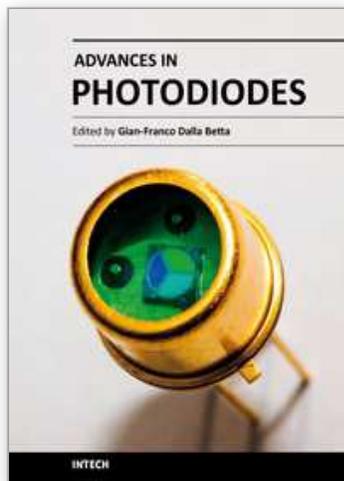
Table. 3. Key measured pixel parameters and improvements

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