We are IntechOpen, the world's leading publisher of Open Access books Built by scientists, for scientists

6,900
Open access books available

185,000
International authors and editors

200M
Downloads

Our authors are among the

154
Countries delivered to

TOP 1%
most cited scientists

12.2%
Contributors from top 500 universities



WEB OF SCIENCE™

Selection of our books indexed in the Book Citation Index in Web of Science™ Core Collection (BKCI)

Interested in publishing with us?
Contact book.department@intechopen.com

Numbers displayed above are based on latest data collected.
For more information visit www.intechopen.com



4

Evolutionary Memory: Unified Random Access Memory (URAM)

Yang-Kyu Choi and Jin-Woo Han
Korea Advanced Institute of Science and Technology (KAIST)
Republic of Korea

1. Introduction

Over the course of the past three decades, we have witnessed dramatic changes in our lifestyles. This is attributed to an unprecedented revolution of information technology (IT). The key element of the IT revolution is the continuing advancement of semiconductor technology. A major driving force of semiconductor technology lies in silicon. The silicon semiconductor has been applied to logic chips as well as memory chips for various applications. Meanwhile, the silicon memory has been at the center of an ongoing battle to manufacture the smallest, highest density, and most innovative product. Since their invention in the early 1970s, silicon memory devices have advanced at a remarkable pace. Silicon based memories such as dynamic random access memory (DRAM), static random access memory (SRAM), and Flash memory have been crucial elements for the semiconductor chip industry in the areas of density, speed, and nonvolatility, respectively. An important growth engine is scaling, which has enabled multiple devices to be integrated within a given area, resulting in an exponential increase in density and a decrease in bit-cost (Moore, 1965). The traditional scaling approach, however, is now confronting physical and technical challenges toward the end-point of the international technology roadmap for semiconductors (ITRS), indicating that the revenue from downscaling will diminish as scaling slows. Thus, an entirely new concept is required to ensure that silicon memory technology remains competitive. To meet this stringent requirement, this chapter will exploit a new paradigm of memory technology.

An ideal memory device should satisfy three requirements: high speed, high density, and nonvolatility. Unfortunately, a memory satisfying all requirements has yet to be developed. Memory devices have consequently been advanced by pursuing just one of these virtues, and appear in many different forms. SRAM dominates high speed on-chip caches for advanced logic and DRAM occupies applications for high-density and high-speed computation; but DRAM's data is volatile, and Flash memory is widely used for high density and non-volatile data storage. Therefore, if a single memory transistor can process different memory functions, a paradigm shift from 'scaling' to 'multifunction' can continue the evolution of silicon technology. In this chapter, the prototype of the fusion memory, named unified-random access memory (URAM), is introduced that can simplify device architecture, reduce power consumption, increase performance, and cut bit-cost.

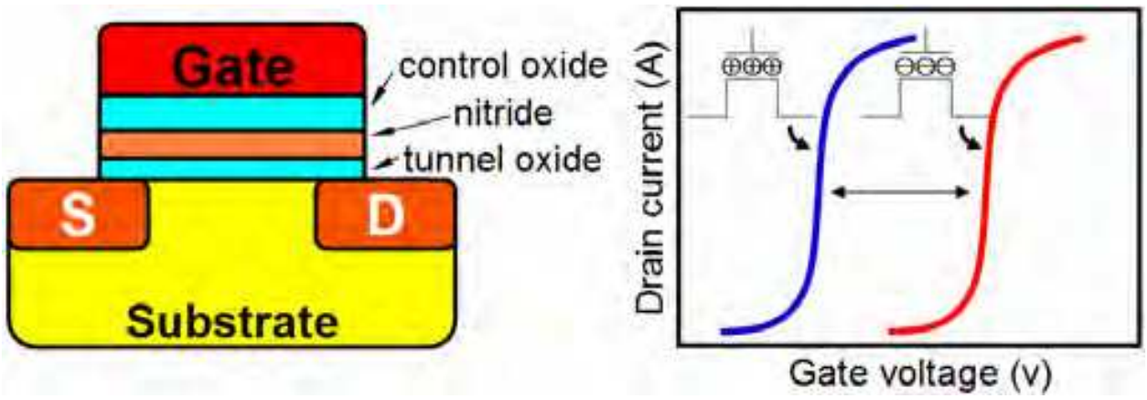
Source: Advances in Solid State Circuits Technologies, Book edited by: Paul K. Chu,
ISBN 978-953-307-086-5, pp. 446, April 2010, INTECH, Croatia, downloaded from SCIYO.COM

2. Operational principle of URAM

URAM is composed of a single memory transistor, which must be of the smallest cell size. It can perform nonvolatile functions or high-speed operations according to the set of operational biases. In other words, circuit designers can specify URAM to be Flash memory or DRAM in order to comply with their specifications. Before discussing the details of URAM, each underlying operation principle is briefly introduced.

2.1 Flash memory operation

Advancements in high quality and ultra-thin oxides have paved the way for nonvolatile memory for silicon-oxide-nitride-oxide-silicon (SONOS) devices, which have replaced conventional floating-gate memory (Brown & Brewer, 1998). Fig. 2-1 shows the SONOS device structure and the program/erase operations. The device has a multiple gate dielectric stack consisting of tunnel oxide/nitride/control oxide (O/N/O), and the charges are stored in discrete traps in the nitride layer sandwiched between the upper/lower oxide barriers. The stored charges are positive or negative depending on whether negative or positive voltage is applied to the gate electrode. If positive programming voltage is applied to the gate, the electrons quantum-mechanically tunnel from the inverted channel through the tunnel oxide, and these electrons are stored in the deep-level traps in the nitride layer. During erasing, the holes are injected into the traps in the nitride in a manner similar to the program operation. The data is identified by the difference in the drain current. Once the charges are stored, the information is retained for up to 10 years with 10^6 to 10^7 program/erase cycles. Due to the superior ability of data retention, SONOS memory is called nonvolatile memory. From the perspective of speed, however, the writing requires few to few tens of microseconds, which might be too long to transfer high density data. Thus, the SONOS has been mainly utilized for portable applications, such as MP3 players, digital cameras, and memory stick solution.

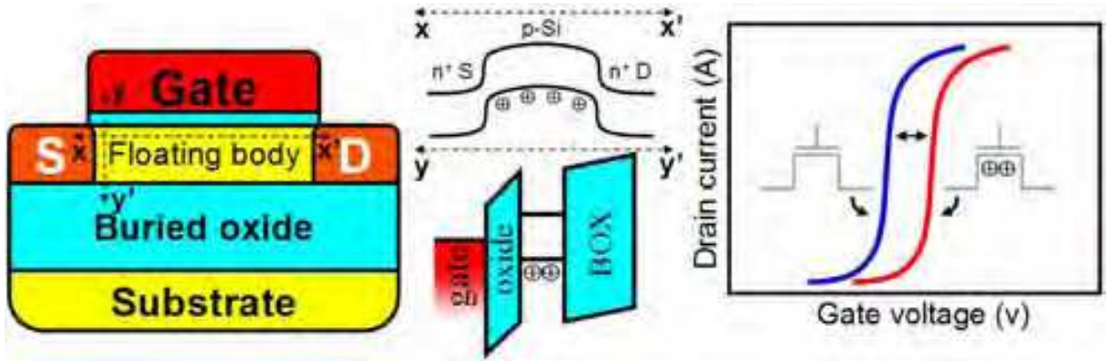


(a) (b)

Fig. 2-1. Operational principle of a SONOS Flash memory. (a) schematic of SONOS structure and (b) drain current versus gate voltage characteristics for two data states. The information is stored as a form of nitride trapped charges. The polarity and amount of charges stored in nitride layer determine the threshold voltages. The data is distinguished by measuring drain current flow at a given voltage. Once the charges are stored, the data is retained for over ten years so that the Flash memory is referred as nonvolatile memory.

2.2 Capacitorless 1T-DRAM operation

In conventional one transistor/one capacitor DRAM (1T/1C DRAM), *Moore's Law* tends to be invalid as the device scaling advances. While the cell transistors continue scaling, the cell capacitors cannot shrink much because they should store a detectable amount of charge, which is equivalent to the minimum cell capacitance, 30fF/cell. Therefore, the size mismatch between the transistors and capacitors leads to complexity in the fabrication process. In 2001 (Okhonin et al., 2001), the densest and cheapest DRAM, which is called capacitorless 1T-DRAM or zero-capacitorless RAM (ZRAM), was developed. The capacitorless 1T-DRAM replaces the large and complicated capacitor to be fabricated with a floating-body capacitor. The capacitorless 1T-DRAM exploits inherent properties, known as the floating body effects or history effects, of transistors made on silicon-on-insulator (SOI) substrates. The floating body effects are generally considered as parasitic by circuit designers because they cause the current overshoot, and obstruct to model and implement into circuit simulator (Gautier, 1997). While the majority of efforts are made to suppress these effects, Okhonin *et al*. found out that they can be a method to temporarily store the information. Fig. 2-2 illustrates the principle of the capacitorless 1T-DRAM. In the program, the impact ionization process generates pairs of electron and holes. While the electrons exit the channel through the drain, the holes are repelled by the drain, charging the body. Since the body is isolated vertically by the energy band offset of the buried-oxide and gate oxide, and laterally by the built-in potential energy of the n^+ source and n^+ drain with a p-type body, the confined holes are stored inside the floating body, as shown in Fig. 2-2. During erase, the negative drain voltage pulls the holes out of the floating body. The information is identified by turning on the transistor and measuring the amount of current flow. More current flows at programmed state as the positive body charges contribute to lowering the channel potential. Since the holes can disappear by recombination at the programmed state and the holes can be generated by band-to-band tunneling or thermal generation at the erased state, the data is volatile. However, as the generation and removal of holes only takes a few nanoseconds, the capacitorless 1T-DRAM can be embedded for high-speed applications such as the caches of microprocessor, digital signal processor (DSP), system-on-chip (SOC), *etc*.

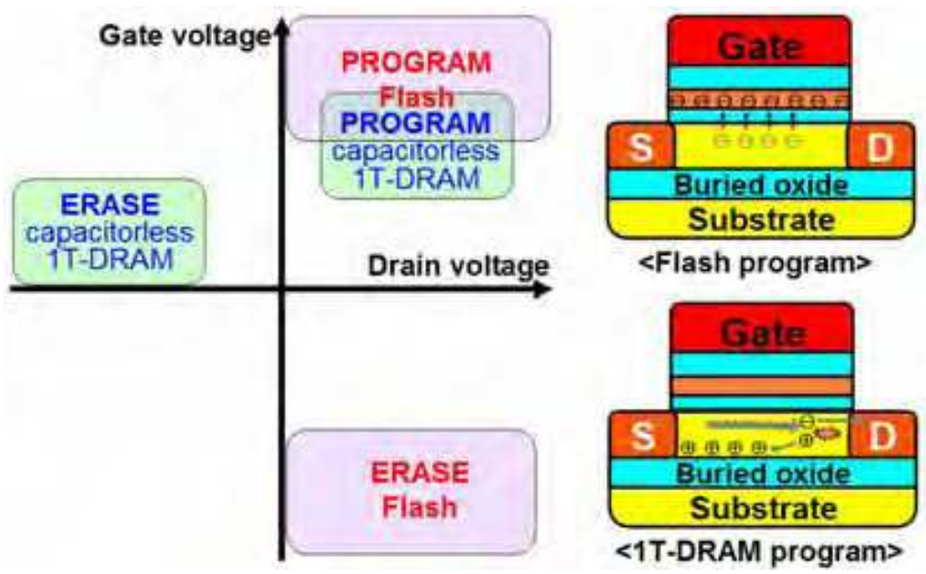


(a) (b) (c)

Fig. 2-2. Operational principle of a capacitorless 1T-DRAM. (a) Schematic of floating body structure, (b) energy band diagram of capacitorless 1T-DRAM, and (c) drain current versus gate voltage characteristics for two data states. The information is stored as a form of floating body charges. The excess holes inside the floating body increase the drain current. Since the stored charges disappear in a second, it is referred as DRAM.

2.3 Operation principle of URAM

The basis of URAM lies in the difference of the inherent operational biases for Flash and capacitorless 1T-DRAM (Han et al., 2007). Fig. 2-3 shows an operational bias domain for two memory modes. For erase operation, the two erase bias regions are distinctive. For program operation, even though the two regions partially overlap, the Flash memory utilizes relatively higher biases than the capacitorless 1T-DRAM. The overlapping region might cause them to disturb each other, a problem that will be solved in Section 5. If the proper biases are selected, two functions can work without disturbance from each other. In order to realize two functions in a single transistor, O/N/O gate dielectric is embodied onto a floating body transistor. When the Flash memory mode is activated, relatively higher voltages are used. On the other hand, relatively lower voltages are utilized to activate the capacitorless 1T-DRAM mode. Once the mode of URAM is determined, the operational biases are accordingly selected.



(a) (b)

Fig. 2-3. (a) Operational bias domain of URAM and (b) schematics device structure and the program mechanism of two functions. The inherent difference stems from the distinctive operational domain, which allows independent functions in a single memory transistor.

The operational sequence is presented in Fig. 2-4. The memory block is firstly selected, and the operation mode is then decided. If the nonvolatile mode is chosen, the Flash operation is activated. Similarly, the capacitorless 1T-DRAM is activated if the high speed mode is needed. When the mode transits from Flash to capacitorless 1T-DRAM, the cell transistors in the selected block should be initialized to have a threshold voltage of 0.2V. If the threshold voltages are not initialized and high value remains, the greater gate voltage would be required to bias the fixed gate overdrive voltage. The high gate voltage can gradually impose stress on the gate oxide, which gradually increases the threshold voltage. On the other hand, if the initialized threshold voltage is small or even negative, excess holes can be generated, even in the zero gate voltage (off-state) since the carrier supplement is sufficient to trigger impact ionization, which can cause drain disturbance. It should be noted that the impact ionization process for the program operation of the capacitorless 1T-DRAM can

adversely affect the charge trapping into the O/N/O layer. Here, the undesirable threshold voltage shift caused by capacitorless 1T-DRAM program is referred to as a soft-program. Since the soft-program causes unstable operation, the threshold voltage should be periodically monitored to find out whether the cells have suffered from soft-programming. The memory block would be re-initialized if the cells failed the verification test. This verification and re-initialization loop is an essential but time consuming process. The method to minimize and, furthermore, eliminate this redundant loop will be discussed in Section 5.

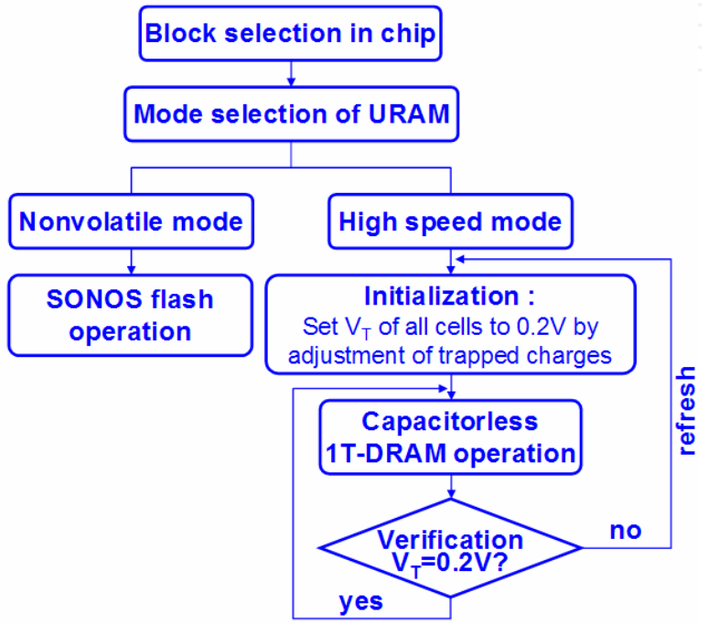


Fig. 2-4. Operational sequence diagram for URAM. The mode is selected according to the designer's demand. Since the program mechanism between two modes partially overlaps, the verification and re-initialization loop is inserted in high-speed mode.

3. Device fabrication and various quantum substrates

3.1 Various quantum substrates for URAM

To date, silicon-on-insulator (SOI) substrate has been utilized for the capacitorless 1T-DRAM. As embedded DRAM (eDRAM) now occupies more than 50% of the total chip area, and advanced processors have started to pick up SOI, the capacitorless 1T-DRAM made on SOI substrate is highly attractive for embedded memory. However, since a bulk substrate still occupies a significant portion of the market share, if the floating body effect is found in the bulk substrate, a chip built on the bulk substrate will be fully blessed with the benefits from the bulk substrate technology. It is true that major memory industries are conservative to adopt SOI substrate for their stand-alone memory products mainly due to the cost issue. Therefore, the capacitorless 1T-DRAM fabricated on the bulk substrates will be explored in terms of not only the embedded memory, but also stand-alone memory applications. In this section, the various quantum substrates, in particular the bulk substrates embodied with the quantum energy band structure, are introduced and the device fabrication process is illustrated.

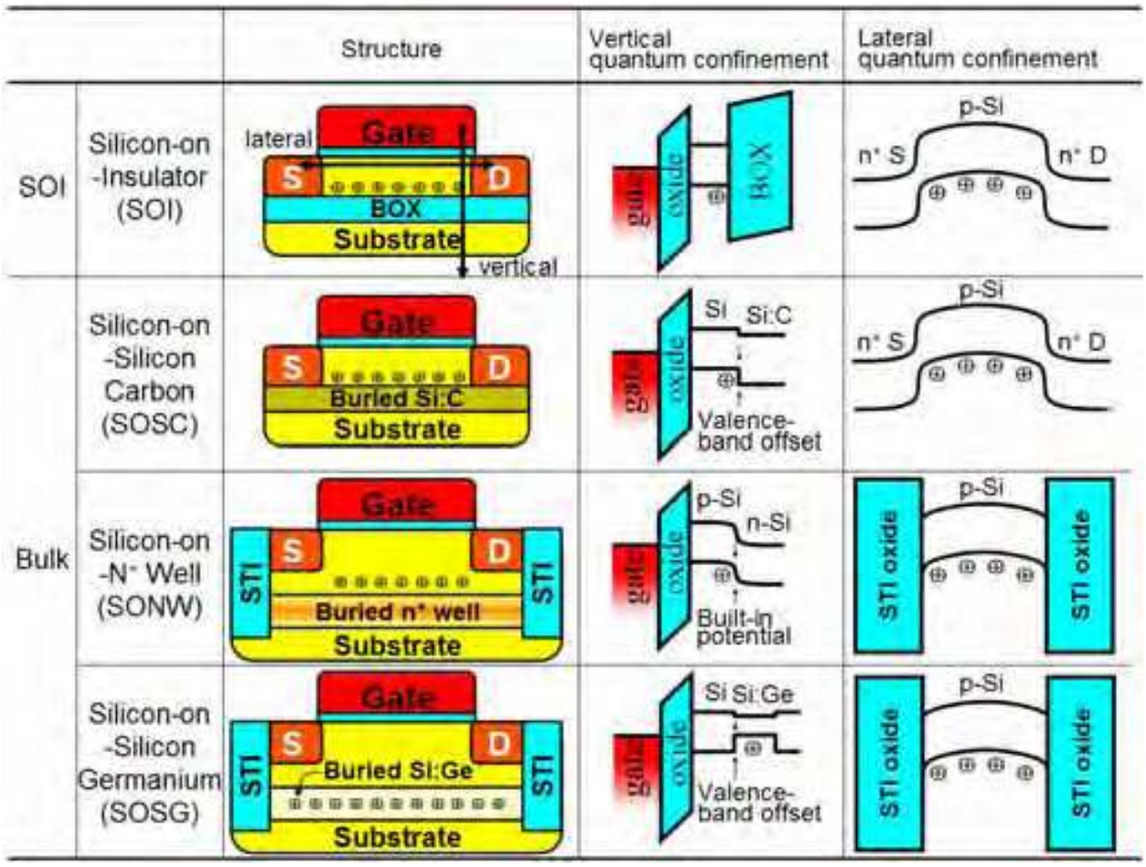


Fig. 3-1. Various templates and their energy band diagrams for excess hole storage. The SOI, SOSC, and SONW are potential barrier types, and the SOSC is potential well types. Unlike the SOI and SOSC, the SONW and SOSG confine holes by shallow trench isolation (STI) oxide in the lateral direction.

The quantum substrates used for the device fabrication and their corresponding energy band diagram for hole storage are comparatively shown in Fig. 3-1. In SOI substrate, the excess holes are vertically confined between the tunnel oxide and the buried oxide and are horizontally isolated by the built-in potential barrier of the n^+ source/drain and p-type body. Next, three methods for the floating body in bulk substrates are introduced. The hetero-epitaxial growth of semiconductor can imitate the energy band lineup of SOI. The introduction of carbon (C) into the silicon substrate enlarges the energy band-gap (Kim & Osten, 1997). Thus, the sequential growth of $Si_{1-y}C_y$ and Si on the bulk wafer can mimic SOI substrate. Here, $Si_{1-y}C_y$ serves as the role of the buried oxide. This substrate is named SOSC after the abbreviation of silicon-on-silicon carbon. Similar to the SOI substrate, the tunnel oxide and the valence band barrier at $Si/Si_{1-y}C_y$ confine holes in the vertical direction, and the built-in potential at the junction boundary confines in the horizontal direction. The n^+ ion deep implantation onto the p-type bulk substrates forms the buried n-type well structure (Ranica et al., 2005). The n-type well and p-type body forms a built-in potential barrier that prevents the holes from flowing out to the substrate terminal. This template is named SONW after the abbreviation of silicon-on-n^+ well. Whereas the holes are horizontally isolated by the junction barrier at SOI and SOSC, the SONW confines hole by

shallow trench isolation (STI) oxide. In order to an avoid electrical short between the n^+ source/drain and n^+ well, the n^+ well should be buried much deeper than the junction depth of the source/drain. This requirement inevitably imposes a minimum space between the two junctions. Therefore, that opened space should be filled by the STI oxide. The aforementioned three substrates: SOI, SOSC, and SONW, vertically confine holes with the potential barrier. Similarly, a potential well can also store the excess holes as the potential barrier did. Similar to the SOSC preparation, the introduction of germanium (Ge) into the silicon substrate reduces the energy bandgap. Thus, the sequential epitaxial growth of $Si_{1-x}Ge_x$ and Si forms the potential well (Ni & Hansson, 1990). In order to avoid the loss of the excess holes via recombination at the source/drain junction, buried $Si_{1-x}Ge_x$ is placed under the source/drain junction boundary. As a result, the STI oxide blocks the evacuation of stored holes along the lateral direction. The silicon-on-silicon germanium is referred to SOSG. In addition to the fundamental interest in the well-type storage media, $Si_{1-x}Ge_x$ is more frequently studied in the literature than $Si_{1-y}C_y$, and $Si_{1-x}Ge_x$ has been already adopted for the strained technology in the mass production so that SOSG technology might be more practical.

3.2 Device fabrication

There are two common types of Flash memory array architectures: NAND and NOR which follow to the logical form of the cell configuration. The cell layout of URAM is the same as that of NOR type Flash because the drain voltage should be applied to each memory cell to trigger the impact ionization. The cell layout of URAM is shown in Fig. 3-2. The gates of each cell are coupled by a row line, and their drains are coupled with column lines. Since the individual memory cells are connected in parallel, random access is allowed. NOR architecture generally has one contact per two neighboring cells by sharing the source contact, thereby reducing the chip area. Some types of URAM, however, cannot use the shared source contact. While the shared source is possible for SOI and SOSC, SONW and SOSG require each source contact for all cells because each cell should be isolated by the STI oxide. The cross-sectional schematic along the bit-line direction in Fig. 3-3 shows that the source can be shared in SOI and SOSC. If the source is shared at SONW and SOSG, however, the lateral migration of excess holes can disturb the body charges of the neighboured cell. In other words, every cell should be isolated by the STI oxide and have their own source line. As a result, the layout efficiency of SOI and SOSC is better than that of SONW and SOSG.

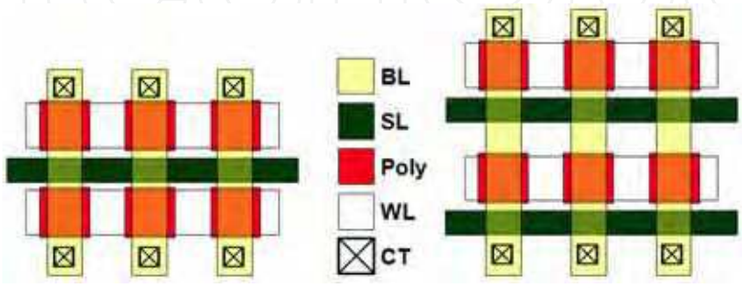


Fig. 3-2. Two types of URAM configuration. (a) Shared source line uses one contact for two cells and (b) divided source lines require individual contact for each cell.

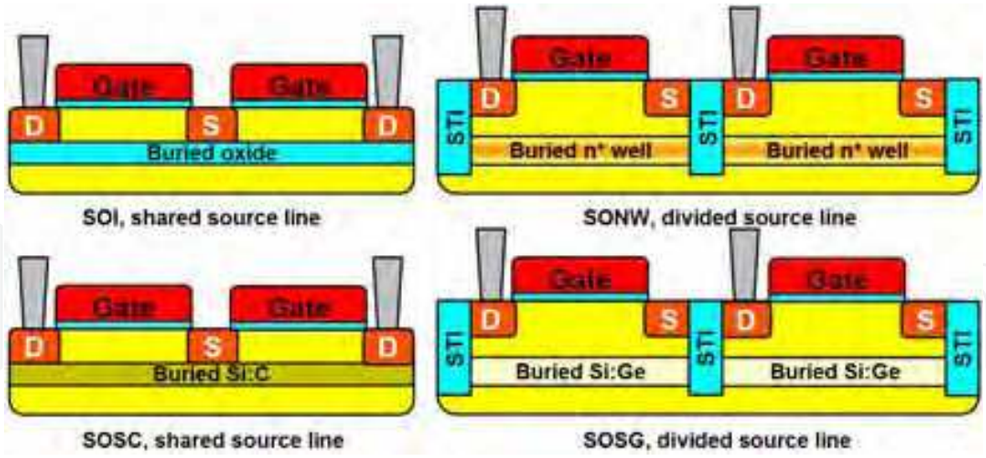


Fig. 3-3. Schematics of the cells along the word line direction. Whereas the SOI and SOSC use the shored bit line, the SONW and SOSG should utilize the divided source line.

The schematic of the process flow is shown in Fig. 3-4 (Han et al., 2009). Except the SOI substrate, SOSC, SONW, and SOSG utilize the bulk silicon wafer. Whereas SOI itself provides the intrinsic floating body, bulk substrates require the energy band engineering to form the extrinsic floating body. The n^+ deep ion implantation is carried out for the SONW, $Si_{1-y}C_y/Si$ is epitaxially grown for SOSC, and $Si_{1-x}Ge_x/Si$ is epitaxially grown for SOSG. After the various types of the templates are prepared, the subsequent processes are similar. A photolithography process with a 0.18μm design rule is applied for channel definition. The photoresist is then trimmed down to a line width of 30nm by plasma ashing. The silicon is etched by reactive ion etching (RIE), resulting in the a 30nm width fin shaped channel. High density plasma (HDP) oxide is deposited and planarized by chemical mechanical polishing (CMP) and partially recessed by diluted HF until the upper part of the fin is exposed. The remaining lower part of the fin is covered by the isolation STI oxide, and the exposed upper part of the fin becomes the active area. The gate dielectric stack, tunnelling oxide/nitride/control oxide, is formed, and *in-situ* doped n^+ polysilicon for the gate is sequentially deposited. After the gate patterning, source/drain implantation and activation are carried out followed by forming gas annealing.

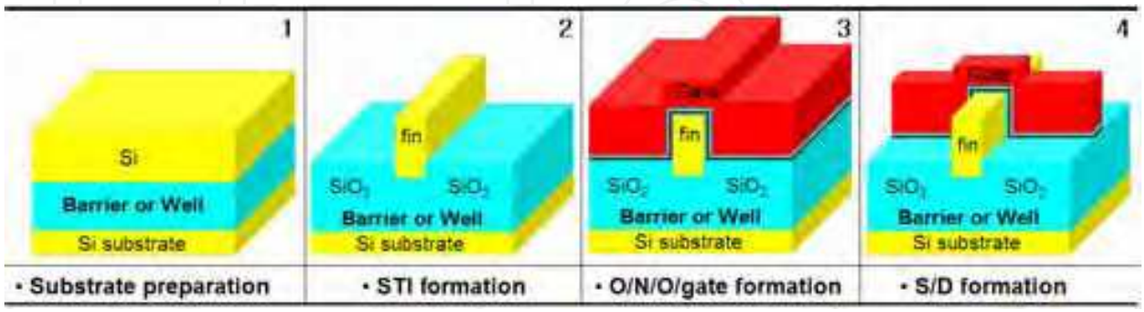


Fig. 3-4. Process flow of the URAM. After the quantum substrates for the floating body are prepared, the subsequent process flow is identical. Whereas SOI itself provides the intrinsic floating body, bulk substrates are hindered by the energy band engineering to form the extrinsic floating body. The n^+ deep ion implantation is carried out for the SONW, $Si_{1-y}C_y/Si$ is epitaxially grown for SOSC, and $Si_{1-x}Ge_x/Si$ is epitaxially grown for SOSG.

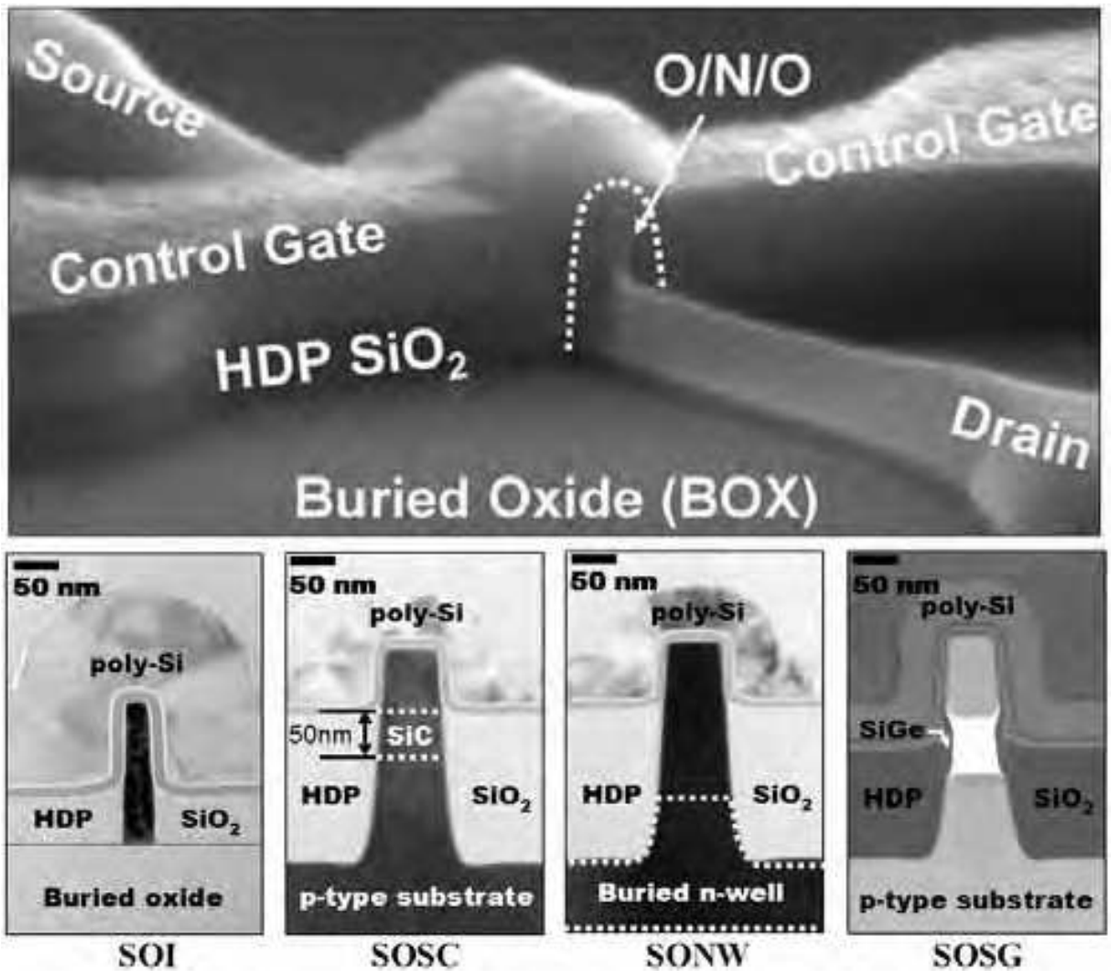


Fig. 3-5. Tilted view of the SOI URAM (upper), and cross-sectional view of four types of URAM (lower).

Tilted scanning electron microscopy (SEM) image and cross-sectional transmission electron microscopy (TEM) images of the fabricated device on various quantum templates are shown in Fig. 3-5. Table 3-1 summarizes the geometric dimensions.

	SOI	SOSC	SONW	SOSG
Gate length	180nm	180nm	180nm	180nm
Fin width	30nm	50nm	50nm	50nm
Fin height	110nm	50nm	100nm	85nm
O/N/O thickness	3/6/3nm	4/6/4nm	4/6/4nm	3/6/4nm
Doping concentration	$5x10^{17}/cm^3$	undoped	$5x10^{18}/cm^3$	undoped

Table 3-1. Summary of geometric dimensions for four types of URAM.

4. Device performance

4.1 Direct Current (DC) characteristics of URAM

Once the devices are fabricated, the fundamental properties should be investigated to find out whether the current-voltage characteristics are acceptable. The drain current (I_D) versus gate voltage (V_G), *i.e.* transfer characteristics, is commonly monitored, providing important parameters such as threshold voltage (V_T), on-current (I_{on}), off-current (I_{off}), subthreshold slope (SS), drain induced barrier lowering (DIBL), *etc*. Fig. 4-1 shows the transfer plot for URAM. The SOI exhibits the steepest SS due to the well known fact that the depletion capacitance is the smallest at SOI. Whereas V_T of the SOI, SOSG, and SOSG are similar, that of the SON is larger than others because of the high body doping concentration. In order to avoid an electrical short between n^+ source/drain and n^+ well, body doping concentration should, reluctantly, be high. Thus, driving current degrades due to the mobility degradation stemming from impurity scattering. It is found that the other parameters are superior to the counter devices (planar single-gate structure), which is attributed to the three-dimensional device structure. The device parameters are summarized in Table 4-1.

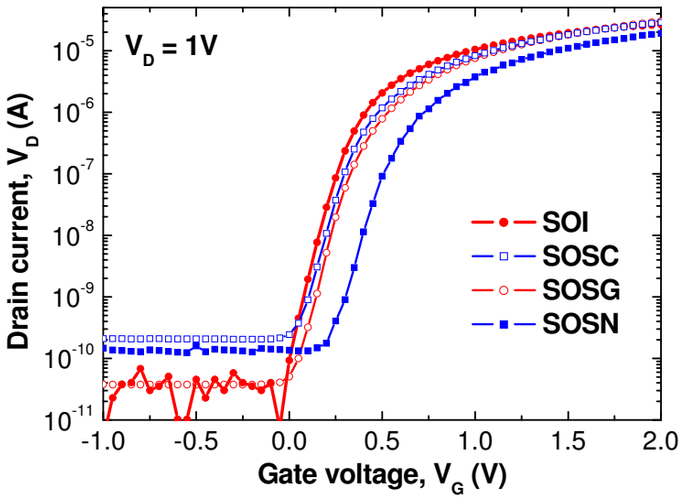


Fig. 4-1. Drain current versus gate voltage characteristics for various types of URAM. The superior device properties are attributed to the three dimensional device structure.

	SOI	SOSC	SOSG	SONW
Threshold voltage	0.21V	0.29V	0.33V	0.5V
Subthreshold slope	85mV/dec	93mV/dec	95mV/dec	101mV/dec
DIBL	32mV/V	110mV/dec	115mV/dec	151mV/dec
On-current	9.3×10^{-11}A	2.4×10^{-10}A	1.3×10^{-10}A	5.1×10^{-11}A
Off-current	1.0×10^{-5}A	8.2×10^{-6}A	3.7×10^{-6}A	7.6×10^{-6}A

Table 4-1. Summary of the device performances. The high threshold voltage in SONW is attributed to the high body doping concentration.

The simplest method to verify whether the impact ionization generates excess holes that will be stored inside the body is to examine the kink point in the drain current (I_D) versus drain voltage (V_D), *i.e.* output characteristics. As the drain voltage increases, the impact ionization process begins to occur beyond a certain drain voltage, generating pairs of electrons and holes. While the generated electrons flow out toward the drain terminal, the generated holes are repulsed to the body by positive drain voltage. In bulk substrates, generally, these holes are collected by a grounded substrate terminal, appearing as a form of substrate current. If the body is electrically floated, however, the holes are accumulated, contributing as an extra quasi-gate. Therefore, the accumulation of excess holes causes current increase at certain drain voltage, and anomalous output characteristics can be found. Fig. 4-2 shows the output characteristics for URAM. The kink points assure that the excess holes are effectively accumulated, even at the bulk substrates, which are quantum mechanically engineered.

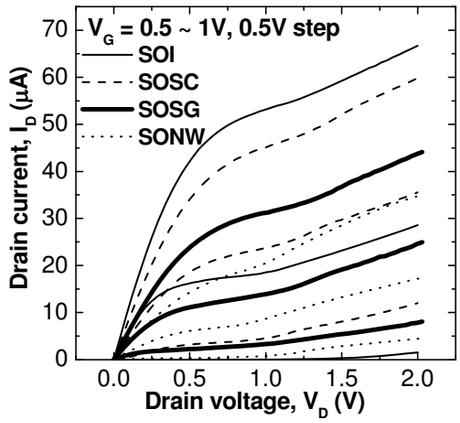
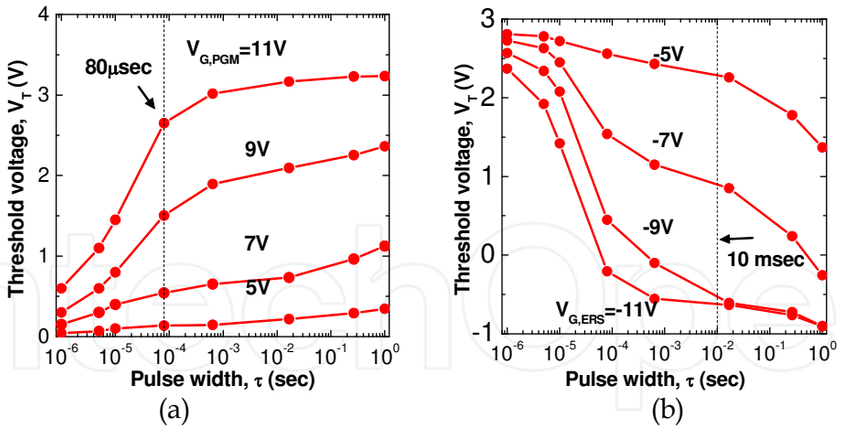


Fig. 4-2. Drain current versus drain voltage characteristics for various types of URAM. As the drain voltage increases, the excess holes generated by the impact ionization are stored in the floating body, resulting in a kink in the saturation region.

4.2 Flash memory characteristics

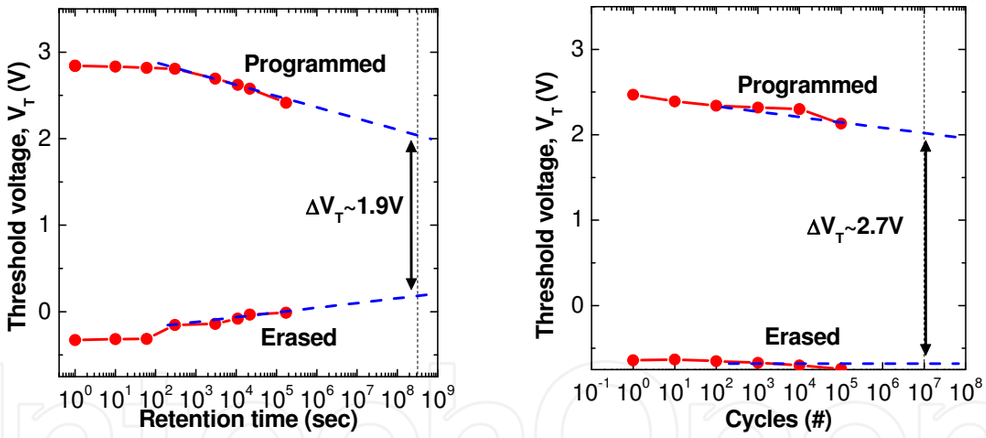
Flash memory performance is normally evaluated in terms of four aspects: program speed, erase speed, data retention time, and endurance cycles. For nonvolatile memory application, the cells should satisfy the 10-years data retention requirement with 10^7 program/erase endurance cycles. The ability to store and recover data after ten years is called 'retention', and the ability to withstand repeated program/erase cycles is called 'endurance'. The program/erase can be carried out by Fowler-Nordheim (FN) tunneling or hot-carrier injection (HCI). In this study, the program/erase is enabled by FN tunneling. Fig. 4-3 shows representative program/erase transient characteristics. The characteristics are obtained from the SOI, representatively. As the program/erase voltages are increased, a higher threshold voltage shift is achieved. In addition, as the program/erase time is increased, the threshold voltage is at first shifted and then saturated after a certain time. Normally, the erase speed is slower than the program speed because the tunneling efficiency of holes is lower than that of electrons due to the high effective mass and energy barrier height in the valence band side. Thus, in a memory array, erase operation is normally carried out by block erasing to improve the erasing throughput. Here, a V_T window of 3.3V is achieved at the program of 11V with 80μsec and the erase of -11V with 10msec.



(a) (b)

Fig. 4-3. Program/erase transient characteristics of Flash memory mode at SOI URAM. (a) program transient and (b) erase transient characteristics. (Han et al., 2007)

The retention and endurance are crucial factors that determine the reliability of the Flash. Fig. 4-4 shows that the 10-years retention and 10^7 cycles are guaranteed with a 1.9V detection window. Table 4-2 summarizes the reliability factors for various templates. No memory retention and endurance failure are obtained as long as the detectable threshold voltage window is greater than 1V. The endurance failure for SOSG is speculated to be caused not by a structure related failure, but by a process induced failure of O/N/O.



(a) (b)

Fig. 4-4. (a) Data retention and (b) endurance characteristics of Flash mode at SOI URAM. (Han et al., 2007)

	SOI	SOSC	SOSG	SON
ΔV_T (11V / 80μsec, -11V / 10msec)	3.3V	3.6V	3.0V	3.6V
ΔV_T (after 10 years)	1.9V	3.5V	2.6V	1.6V
ΔV_T (after 10^7 cycles)	2.7V	3.2V	Fail	2.7V

Table 4-2. Summary of program/erase efficiency and reliability for various types of URAM.

4.3 Capacitorless 1T-DRAM characteristics

A capacitorless 1T-DRAM mode is characterized by the customized system. Fig. 4-5 shows the measurement system. The computer controls the pulse generator (Agilent 81110A), oscilloscope (Agilent 54542C), and current amplifier (Keithley 428). The pulse generator applies voltage patterns to the device. The source current is amplified by the current amplifier, changed into a form of voltage, and monitored by the oscilloscope. For low noise measurement, a low noise cable with length of 50cm is used. The device is tested under the probe station (Cascade R4840). All operations utilize the gate voltage of 1V, which is not an indispensable condition, but for monotone waveform to simplify the sensing circuit circuitry.

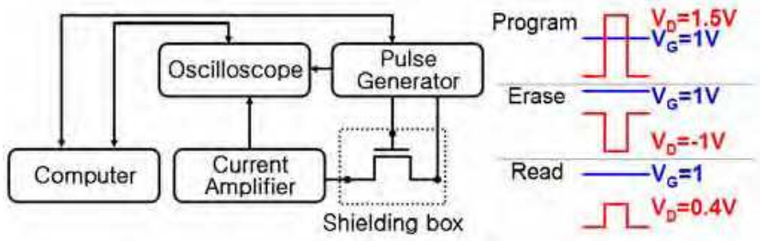
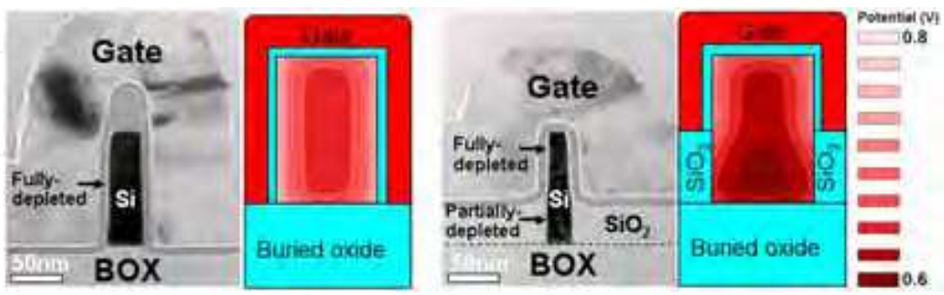


Fig. 4-5. Customized measurement system and the operational pulse waveform.

In order to minimize the leakage paths in the three-dimensional FinFET, the fin width should be as narrow as possible. This means that a fully depleted body is desirable in terms of scalability. The capacitorless 1T-DRAM, however, requires a partially depleted body, *i.e.* wider fin width, to store the detectable amount of holes. To compromise the scalability and the performance functionality, the fin is divided into two regions (Han et al., 2009). Fig. 4-6 compares the conventional FinFET and the proposed one as counterpart structures. Whereas the fin is fully surrounded by the gate at the conventional FinFET, the fin of the proposed one is partially covered. The essence of the proposed one is that the hole accumulation region is spatially separated from the inverted channel. The upper part covered by the gate, which is fully depleted, provides a conduction path. The lower part covered by STI oxide, which is partially depleted, serves for a hole storage. Therefore, scalability and performance functionality (the floating body effect) are attained at the same time.



(a) (b)

Fig. 4-6. Comparative images of (a) the conventional fully-depleted FinFET SONOS and (b) the proposed half fully-depleted and half partially-depleted FinFET SONOS. The contours of the body potential supported by simulation assure that the existence of a partially depleted region to accommodate more holes is attractive for proper 1T-DRAM operation. Consequently, the proposed FinFET is superior to the conventional FinFET. (Han et al., 2007)

Fig. 4-7 shows the program/erase characteristics of the capacitorless 1T-DRAM. As mentioned in Section 2.3, the program/erase voltage should be optimized in order to avoid undesired charge trapping in the O/N/O layer. The program uses $V_{G,PGM}$=1V and $V_{D,PGM}$=1.5V, the erase uses $V_{G,ERS}$=1V and $V_{D,ERS}$=−1V, and the read voltages are $V_{G,READ}$=1V and $V_{D,READ}$=0.4V. Before utilizing the capacitorless 1T-DRAM mode, the initial V_T is set to 0.2 V. The data states are clearly distinguished with a 7μA sensing window after 80msec data retention, whereas the conventional device exhibits a smaller sensing window. This is attributed to the presence of increased excess hole accumulation as shown in Fig. 4-6.

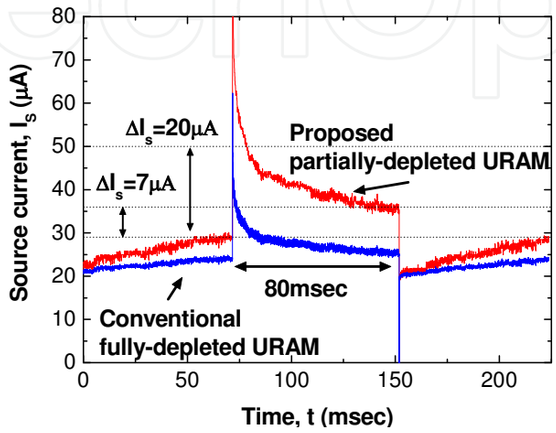
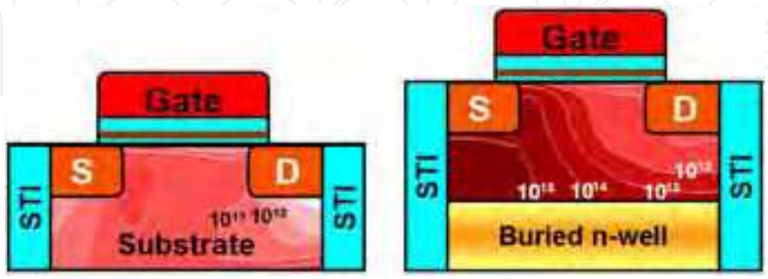


Fig. 4-7. Source current for the capacitorless 1T-DRAM mode. The two data states are clearly identified because more holes are accumulated in the partially-depleted URAM. However, the source current difference is relatively small in the conventional fully-depleted URAM. (Han et al., 2007)

In the SONW substrate, the buried n-type well is embedded inside a p-type bulk substrate. The junction of the p-type body and the n-type well forms the pn built-in potential barrier, thus the excess holes can be retained inside the p-type body region. In order to prove that the excess holes can really be confined, the simulated contours of the hole concentration after the program are shown in Fig. 4-8. In conventional bulk substrates, excess holes are generally collected by the grounded substrate. At the SONW substrate, the holes confront the n-well junction barrier, and the holes are thus accumulated inside the body.



(a) (b)

Fig. 4-8. Simulated contours of the hole concentration biased at hold condition after impact ionization, (a) convention bulk FinFET, and (b) SONW URAM. In contrast to the conventional case, SONW URAM stores the excess holes in the body region. (Han et al., 2008a)

Fig. 4-9 shows the program/erase characteristics. The important feature in the bulk substrates is that the barrier height can be modulated by the substrate voltage. In other words, the ability to retain holes can be improved by proper substrate voltage. An applying a weak positive voltage and enlarging the hole barrier height can enhance the sensing window. The sensing window with retention time is increased from 4μA with 8msec to 7μA with 30msec as the substrate voltage is increased from 0V to 0.3V. In the case of strong positive voltage, however, the capacitorless 1T-DRAM cannot work because the forward biased source/drain to the body junction diode is inevitably turned on.

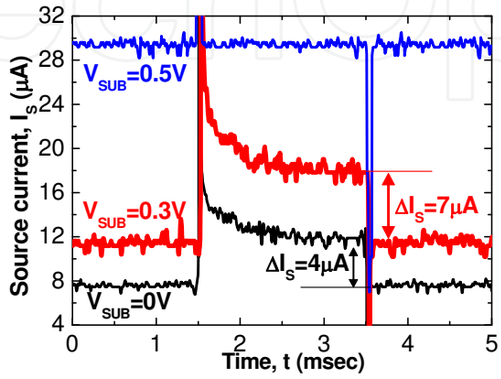


Fig. 4-9. Source current for capacitorless 1T-DRAM of SONW. The sensing window is widened at a small positive substrate voltage. (Han et al., 2008a)

Since the SONW substrate needs the deep implantation process, it is hard to define an accurate and abrupt quantum engineered junction profile. The SOSC would be preferred as its energy band is determined by epitaxial growth and the mole fraction of C in $Si_{1-y}C_y$. In addition, whereas the buried n-well should be located far from the source/drain junction in order to avoid the electrical short, the band offset interface of $Si/Si_{1-y}C_y$ can be at closer to the source/drain so that the influence of stored holes on the inverted channel becomes stronger. Therefore, SOSC gives a rise to improvements in performance. Fig. 4-10 shows the program/erase characteristics. The sensing window of 11μA with a retention time of 50msec at a substrate voltage of 0.3V is wider compared to that of SONW (Han et al., 2008). Also, the sensing window is wider at V_{SUB}=0.3V than at V_{SUB}=0V as predicted.

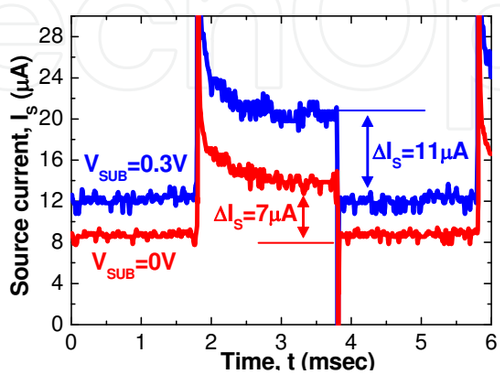
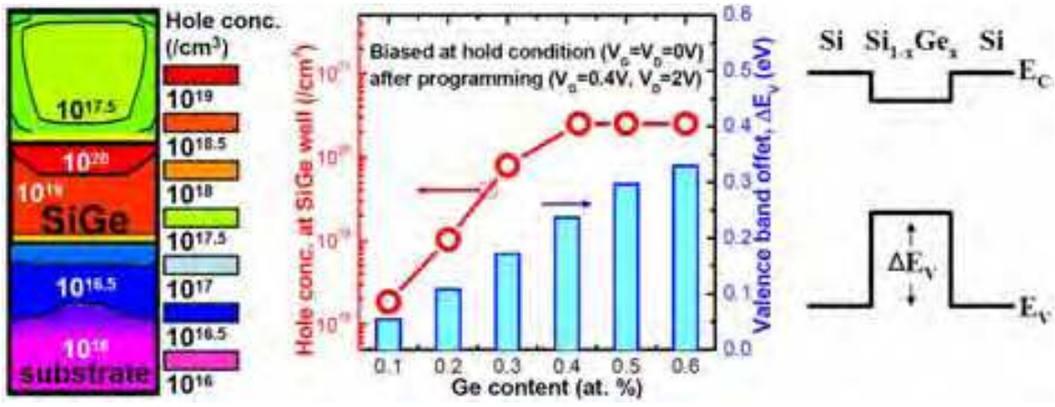


Fig. 4-10. Source current for the capacitorless 1T-DRAM of SOSC. The small positive substrate voltage raises the sensing current window. (Han et al., 2008a)

The above three substrates, SOI, SONW, and SOSC, showed a quantum barrier, *i.e.* the energy band of the floating body is above that of the quantum engineered substrate. In contrast, SOSG is the quantum well structure because the energy band of the floating body is below that of the quantum engineered substrate. The quantum barrier type substrates use their bodies for the conduction path as well as the storage region, simultaneously. This condition can cause the excess holes to easily disappear by recombination with the inverted electrons, leading to degradation in the data retention time. However, the quantum well can separate the excess holes and conduction electrons; thus, the stored charge loss via the recombination process with an inverted electron is expected to be minimized, and improved performance is predicted. The $Si/Si_{1-x}Ge_x/Si$, SOSG, forms the potential well structure because the valence band energy of $Si_{1-x}Ge_x$ is higher than that of Si, as shown in Fig. 4-7. In SOSG, the top Si serves as the conduction channel, and the centered $Si_{1-x}Ge_x$ is devoted to the hole storage region. The major advantage compared to SOSC is that, whereas the solid solubility of carbon in silicon is limited to 5%, the germanium content can be adjusted from 0% to 100%, which allows wide band offset modulation by changing stoichiometry of $Si_{1-x}Ge_x$. Therefore, the SOSG can provide more degrees of freedom in the energy band design because the depth of the potential well is favorably determined by the germanium content. The impact of germanium on the band offset has been theoretically reported, and it turns out that the valence band offset between Si and $Si_{1-x}Ge_x$ is linearly increased with content x. The simulated distribution of excess holes after programming and maximum hole concentration for various content x are shown in Fig. 4-11. The holes are found to be preferentially accumulated in the $Si_{1-x}Ge_x$ layer. The hole concentration is exponentially increased as the valence band offset is increased. However, the hole concentration starts to saturate after a band offset of 0.24eV, which corresponds to germanium content of x=0.4. This means that the usage of Ge higher than x=0.4 will be ineffective in terms of the ability to store holes. In other word, a very deep potential well is not always necessary for higher performance (Han et al., 2008b).



(a) (b) (c)

Fig. 4-11. (a) Simulation results of hole concentration biased at hold condition after impact ionization. The stored excess holes are found in a $Si_{1-x}Ge_x$ potential well, (b) the valence band offset as a function of germanium content and resultant hole concentration, and (c) the energy band offset in the SOSG structure. The amount of stored holes is exponentially increased as the valence band offset is increased, but the hole concentration starts to saturate after a band offset of 0.24eV. (Han et al., 2008b)

Fig. 4-12 shows the program/erase characteristics for two germanium contents, x=0.3 and x=0.5. Despite of the larger sensing window at x=0.5, the retention is found to be inferior to that at x=0.3 due to the fact that the higher defect density caused by an atomic lattice mismatch at x=0.5 induces faster recombination during read operation. In addition to the retention degradation at the programmed state, a deeper potential well also is found to degrade the retention at the erased state. The reason is speculated to be that the holes are easily diffused into the potential well from the neighbored p-type silicon layers, as illustrated in Fig. 4-13. As a result of the trade off between sensing current window and retention time, the optimized stoichiometry of $Si_{1-x}Ge_x$ is x=0.3. The retention time (the order of microseconds) appears to be insufficient to practical application, however, refinement of the epitaxial process and geometric optimization of the 3-D structure will enhance the performance.

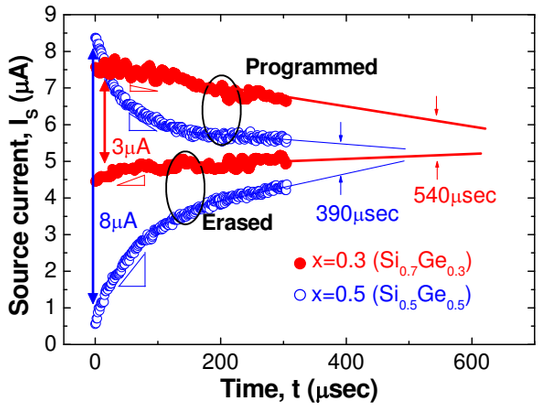
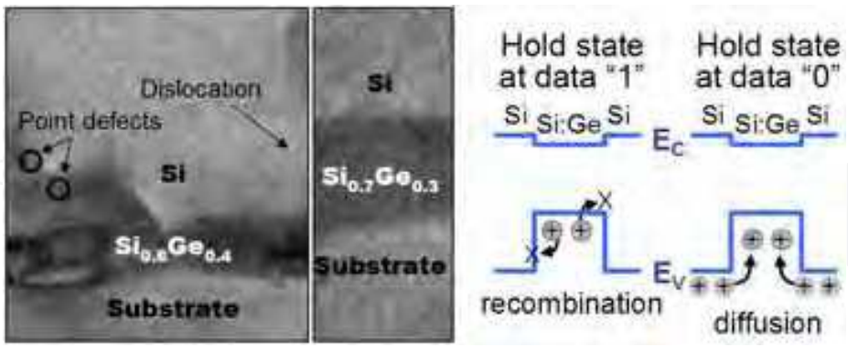


Fig. 4-12. Capacitorless 1T-DRAM characteristics for different germanium content in $Si_{1-x}Ge_x$ of SOSG. The higher x exhibits a wider sensing window at the beginning of the sensing, but also faster charge loss. (Han et al., 2008b)



(a) (b)

Fig. 4-13. (a) Transmission electron microscopy images of x=0.4 and 0.3 and (b) schematics for retention degradation mechanisms. The high germanium content induces a high lattice mismatch because the lattice constant of germanium is larger than that of silicon. The defects originating from the lattice mismatch reduce the data retention at the programmed state via charge recombination, and a deeper potential well degrades the data retention at the erased state due to hole-to-hole repulsion and its repellent diffusion mechanism. (Han et al., 2008b)

Table 4-3 summarizes the features and performances of four types of URAM. The SOI substrate exhibits the fastest write speed, the widest sensing window, and the longest retention among the four substrates. Among the bulk types, the SOSC substrate displays superior performance.

	SOI	SONW	SOSC	SOSG
substrate	SOI	bulk	bulk	bulk
energy band type	valence band barrier	built-in potential	valence band barrier	valence band well
energy band abruptness	abrupt	gradual	abrupt	abrupt
band offset / built-in potential	4.8 eV	0.9 eV	0.18 eV	0.05~0.32eV
channel and storage region	share	separate	share	separate
program speed	6 nsec	20 nsec	20 nsec	50 nsec
sensing window	~20 μA	~7 μA	~11 μA	~8 μA
retention time	~ 80 msec	~ 30 msec	~ 50 msec	~ 600 μsec

Table 4-3. Summary of the features and performance of various URAMs. All data were measured at 300K.

5. Soft-programming issue and solutions

5.1 Soft-programming issue

URAM can be realized by combining the O/N/O gate dielectric to store electrons and the floating body to capture holes in a single transistor. Unfortunately, impact ionization for the program of the capacitorless 1T-DRAM can adversely affect the stored charges in the O/N/O layer. This gives a rise to an undesired threshold voltage shift, which is called 'soft-programming'. The strong impact ionization condition provides faster program speed, a wider sensing window, and longer retention time, but this simultaneously increases the hot-electron injection into O/N/O, leading to instability as a result of the disturbance between the Flash and capacitorless 1T-DRAM modes. Thus, the program condition of capacitorless 1T-DRAM has reluctantly been bounded in order not to disturb the Flash memory states. This is becoming an increasingly important concern.

In order to clarify the soft-programming, Fig. 5-1 shows the capacitorless 1T-DRAM performance after 10^5 cyclic operations. When the drain voltage for a program is 1.8V, a sensing current window of 6μA is sustained, which means the interference is negligible. To improve the performance, when the drain voltage is increased to 2.2V, hot-electron injection is unpropitiously caused. This causes a gradual charge trapping into O/N/O, and the resultant sensing window is decreased. Therefore, a soft-program poses a constraint on the maximum program voltage. In order to overcome this issue, soft-programming immune device structures and operational methods are suggested in the following subsections.

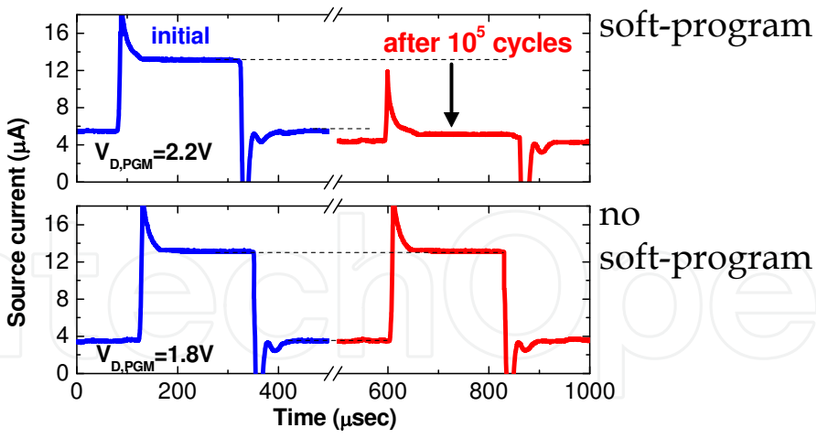
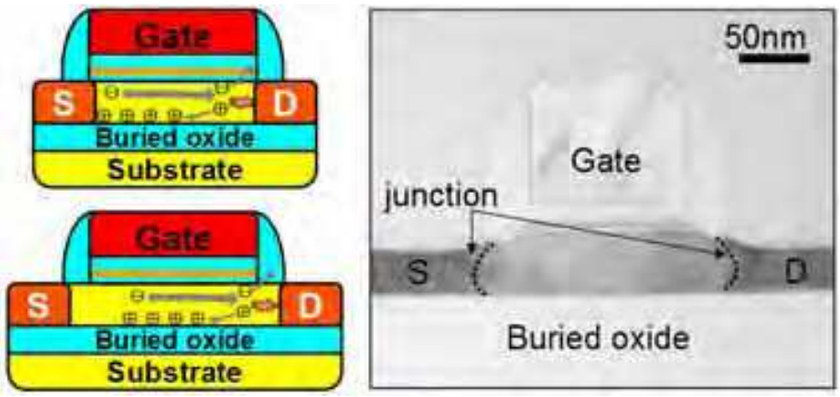


Fig. 5-1. Program/erase characteristics by the impact ionization method for different program voltages. The sensing window is reduced at a high drain voltage as the stress cycles increase due to hot electron injection into the nitride layer. (Han et al., 2009a)

5.2 Soft-programming immune structure: gate-to-S/D nonoverlap structure

The soft-program tends to occur as the impact ionization process is triggered under the gate. Thus, if the impact ionization region is steered out of the O/N/O layer, hot electron injection can be mitigated. The impact ionization process occurs at the region with the highest electric field, *i.e.*, drain end. Thus, a gate-to-source/drain nonoverlap creates an impact ionization region located outside of the gate. Even though the impact ionization triggers a hot-electron injection, the charge trapping is alleviated since there are no trap sites. Thus, the constraint of program bias is relieved. For this purpose, junction nonoverlap structure is fabricated and compared to the conventional overlap structure. Fig. 5-2 shows the fabricated device images. The nonoverlap length is 20nm.

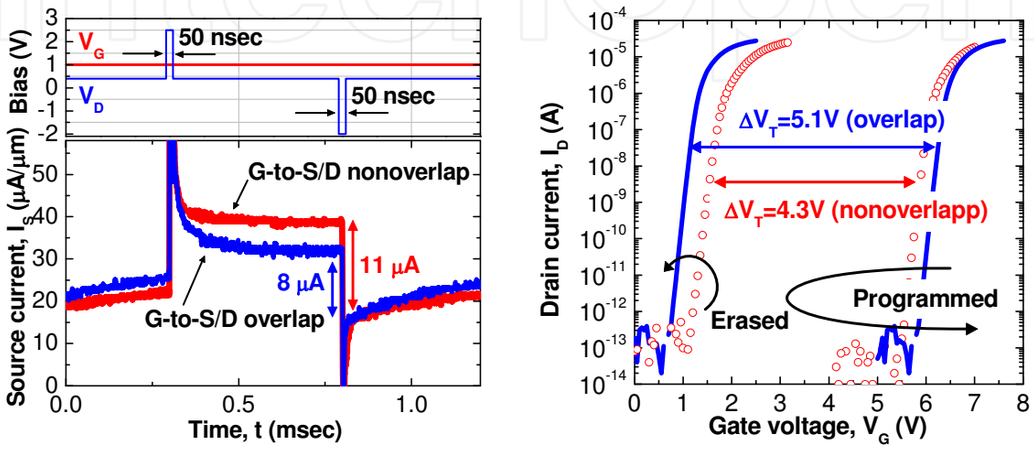


(a) (b)

Fig. 5-2. (a) Schematics of gate-to-source/drain overlap and nonoverlap structure and (b) transmission electron microscopy image of the gate-to-source/drain nonoverlap devices. The body thickness is 50nm, the gate length is 110nm, and the nonoverlap length is 20nm. (Han et al., 2009a)

Fig. 5-3 shows the memory characteristics for both structures. Even though the nonoverlap device may suffer from degradation in the impact ionization efficiency, the sensing current

window of the nonoverlap device is found to be wider than that of an overlap one (Fig. 5-3a) because the nonoverlap reduces the junction leakage and recombination rate. In addition, the effective volume of the floating body is extended by the amount of nonoverlap. As a result, reduced impact ionization efficiency can be compromised (Song et. al., 2008). In the Flash memory characteristics shown in Fig. 5-3b, a threshold voltage window of 4.3V is achieved. The threshold voltage for a fresh device is higher in a nonoverlap than at an overlap device, and the threshold voltage window of a nonoverlap structure is narrower than that of an overlap structure. Despite of the degradation in the threshold voltage window for flash memory, the window of 4.3V is acceptable to identify the data states (Han et al., 2009).



(a) (b)

Fig. 5-3. (a) Capacitorless 1T-DRAM and (b) Flash memory characteristics. The nonoverlap structure shows a wider sensing current window in capacitorless 1T-DRAM mode, but narrow threshold voltage window in Flash mode. (Han et al., 2009a)

In order to evaluate the soft-programming immunity, a stress test is carried out. While the program voltage is applied, the threshold voltage shift is periodically monitored during the operation cycles. As shown in Fig. 5-4, whereas the overlap structure shows a threshold voltage shift of 0.2V, the nonoverlap device exhibits distinctively superior immunity against the soft-program to the overlap device.

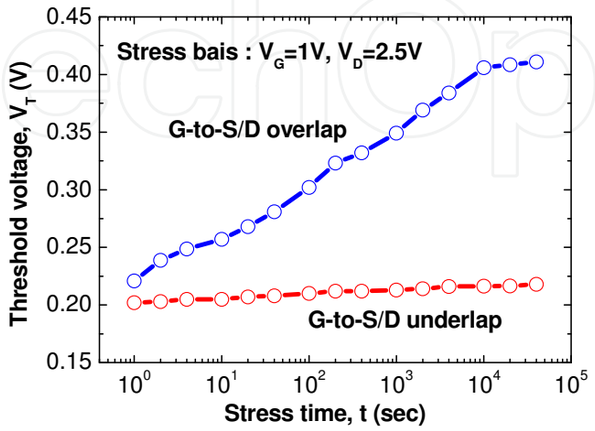
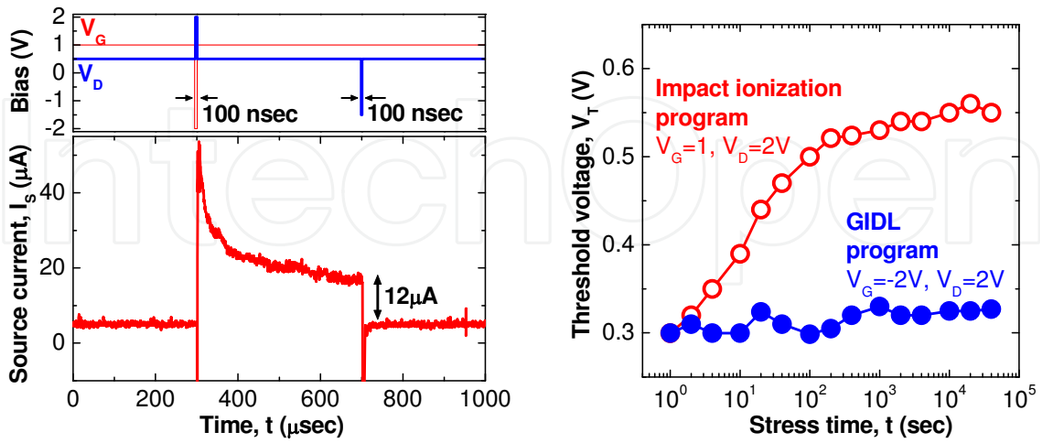


Fig. 5-4. The threshold voltage shift monitored during the cyclic operations. The nonoverlap structure shows superior immunity against the soft-program. (Han et al., 2009a)

It is worthwhile to note that the major weakness of the nonoverlap junction structure is that the parasitic voltage drops via series resistance at the nonoverlap region reduces the impact ionization efficiency. This drawback can be countervailed by increasing the dielectric constant of the gate offset spacer. The high dielectric constant of the spacer can increase the effect of the gate fringing field to the nonoverlap region, which is expected to boost the impact ionization rate (Ma et. al., 2007). Therefore, the abundance of excess holes can further improve the current drivability and recover performance of the capacitorless 1T-DRAM against the sacrificed impact ionization efficiency.

5.3 Soft-programming immune operation: gate-induced-drain-leakage program

To date, impact ionization was commonly used to create excess holes in the body. However, in place of the impact ionization, there is another method to generate excess holes; the gate-induced-drain-leakage (GIDL). A device biased on the GIDL condition, *i.e.*, negative gate and positive drain voltage, creates excess holes in the body by band-to-band tunneling. The impact ionization program significantly wastes power since it is triggered by high drain current. However, GIDL current does not require such drain current; thus, low power operation is feasible. If the O/N/O is in the erase saturation state prior to activating the capacitorless 1T-DRAM mode, the hole injection into O/N/O is effectively restricted. In addition, the hole injection is even suppressed because the effective mass and energy band barrier of the hole in the valence band side are high. Fig. 5-5a shows the program/erase pulse waveform of the GIDL program method and resultant sensing current. The current window of 12μA with 50msec data retention facilitates the data sensing. In order to verify the immunity against the soft-program, the stress test is carried out by the impact ionization and GDIL program methods. The amount of trapped charges is evaluated by monitoring the shift of the threshold voltage. Fig. 5-5b shows the impact of cyclic capacitorless 1T-DRAM on the threshold voltage shift. Whereas the impact ionization condition induces the charge trapping and results in a threshold voltage shift, the GIDL method does not. Thus, the GIDL method is the effective tool to achieve a soft-program immune operation (Han et al, 2009).



(a) (b)

Fig. 5-5. (a) Program/erase characteristic of GIDL program method and (b) threshold voltage shift versus cyclic stress time. The GIDL program method does not shift the threshold voltage, while the impact ionization program does. (Han et al., 2009b)

It is worthwhile to note that the GIDL program method in URAM may be inefficient in terms of the generation efficiency of holes. As the Flash memory utilizes O/N/O gate dielectric, such a thick gate dielectric hampers to achievement of sufficient band bending for band-to-band tunneling. Thus, a programming time of 100nsec was used, which would be too long to apply for the embedded system. Since the thickness of O/N/O is no longer scalable to sustain acceptable nonvolatility, a higher gate voltage would be required, but it also poses power issues. In order to overcome this drawback, a p^+ polysilicon gate on the p-type body can be used. Since the flat band voltage difference between p^+ polysilicon and n^+ drain is higher than that of n^+ polysilicon and n^+ drain, a higher GIDL current is induced at a given gate voltage (Lindert et. al, 1996). Therefore, the implementation of the p^+ polysilicon gate can yield improved memory characteristics in the GIDL method.

5.4 High performance and soft-programming immune operation: parasitic BJT read

In the first prototype of URAM, the impact ionization program condition caused a soft-program issue. Next, despite the suppression of the soft-program, the GIDL program tends to sacrifice program efficiency. In summary, both methods have their distinctive strengths as well as weaknesses, simultaneously. In this section, a third method is introduced for improved performance with soft-program free operation. It is important to note that the floating body MOSFET contains a parasitic lateral bipolar junction transistor (BJT) composed of n^+ source, p-type body, and n^+ drain, which correspond to an emitter, base, and collector, respectively. As the p-type body is floated, the BJT with the floating base cannot be activated in the normal MOSFET operational conditions. However, if the high voltage is applied to the drain, the hole injection to the floating base can turn on the parasitic BJT, and the drain current is maintained even though the MOSFET is supposed to be turned off (Chen et. al, 1988). Fig. 5-6 shows the double-sweep transfer characteristics. At a low drain voltage, the normal MOSFET transfer curved is shown, and there is no hysteresis. At high drain voltage, however, the subthreshold slope approaches 0mV/dec at the time of the parasitic BJT activation, and a hysteresis loop is generated. Thus, even at the given read voltage, bistable current-voltage characteristics can be utilized as a single memory transistor, as indicated in the Fig. 5-6 (Okhonin et. al, 2007).

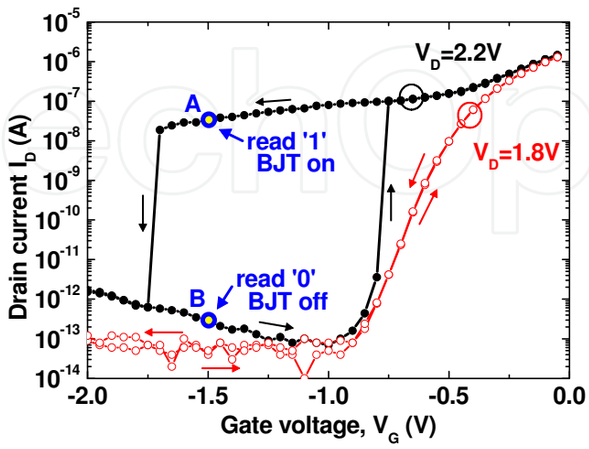


Fig. 5-6. Double sweep drain current versus the gate voltage characteristics at the SOI URAM. At V_D=1.8V, the device shows normal MOSFET transfer characteristics. At V_D=2.2V, the parasitic BJT alternatively begins to work, and the hysteresis loop is created.

Fig. 5-7 comparatively shows the capacitorless 1T-DRAM characteristics with the previous two program methods and the BJT read method. A pulse width of 5nsec is applied for program and erase in the BJT mode. The programming is carried by impact ionization or GIDL, and the erase is fulfilled by forward junction current. The difference lies in the read condition. The previous methods used low drain voltage, typically V_D<0.6V, in order not to disturb the body charged state, resulting in a small sensing current. In addition the sensing current window was gradually narrowed by the generation and recombination processes. In contrast, the parasitic BJT read uses a high drain voltage at least V_D>2V to activate bipolar action. While the negative gate voltage turns off the MOSFET, the parasitic BJT can either be activated or deactivated according to an excessive number of holes or lack of holes. When excess holes exist in the body, a parasitic BJT is activated in which the current corresponds to the point A in Fig. 5-6. On the other hand, when excess holes are eliminated, the parasitic BJT is deactivated, thereby causing the current not to flow, which corresponds to point B in Fig. 5-6. In particular, once the parasitic BJT is activated, the high BJT current is latched despite the MOSFET being in off state because the hole is continuously supplied as long as the read voltage is applied. Therefore, the BJT read method is considered to be completely non-destructive, and the sensing current window is high enough that a sense amplifier may not be necessary to identify the data.

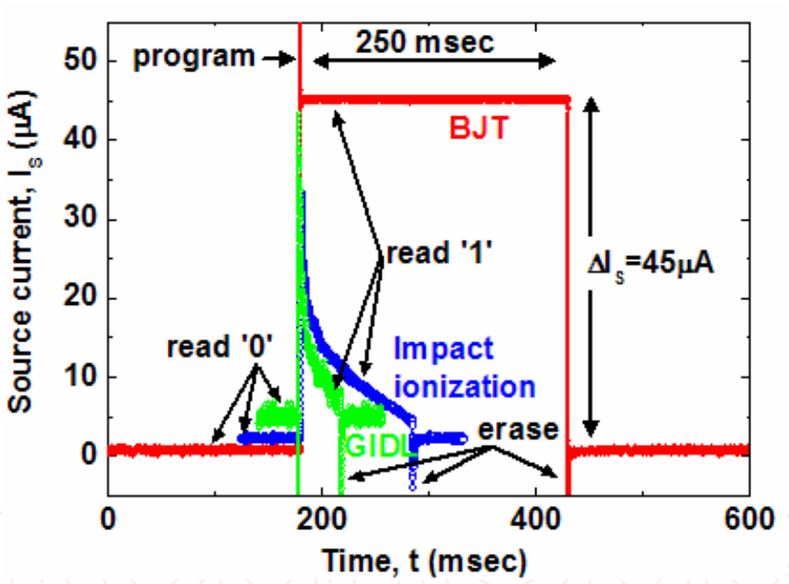


Fig. 5-7. Comparison of the capacitorless 1T-DRAM characteristics with various methods. In the conventional read method, the sensing current window is gradually narrowed with the read time. In the BJT read method, the source current remains constant because the stored data at BJT read condition is latched.

It is important to note that the read and program operations correspond to the hot-hole injection conditions, which can cause a threshold voltage shift during cyclic capacitorless 1T-DRAM operations. This situation seems similar to the soft-program, but it turns out that the soft-program in BJT is negligible, as shown in Fig. 5-8. If the nitride traps are saturated with holes that can be carried out by an initialization step before the capacitorless 1T-DRAM mode, there are no additional threshold voltage shifts because there are no extra available trap sites in the nitride. According to the stress test data, the threshold voltage shift is found

to be negligible, resulting in stable operation. The soft-program free scheme can exclude the operation loop of the verification of the soft-programming and re-initialization that is supposed to be required in the conventional methods, as shown in Fig. 5-9. The elimination of the redundant loop can greatly conserve the integrity of the gate oxide, which can otherwise be degraded by repeated initialization processes.

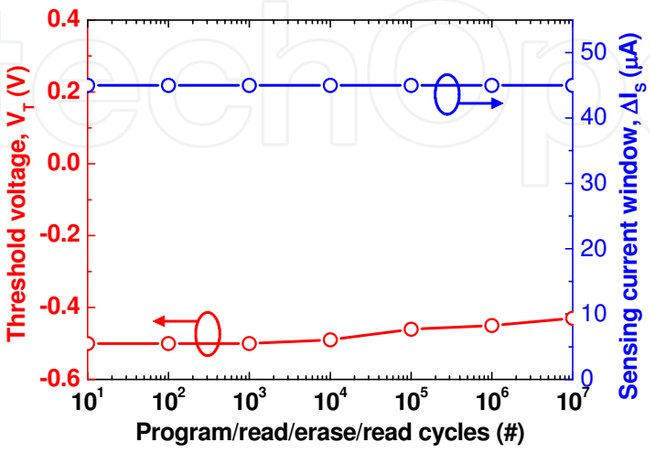
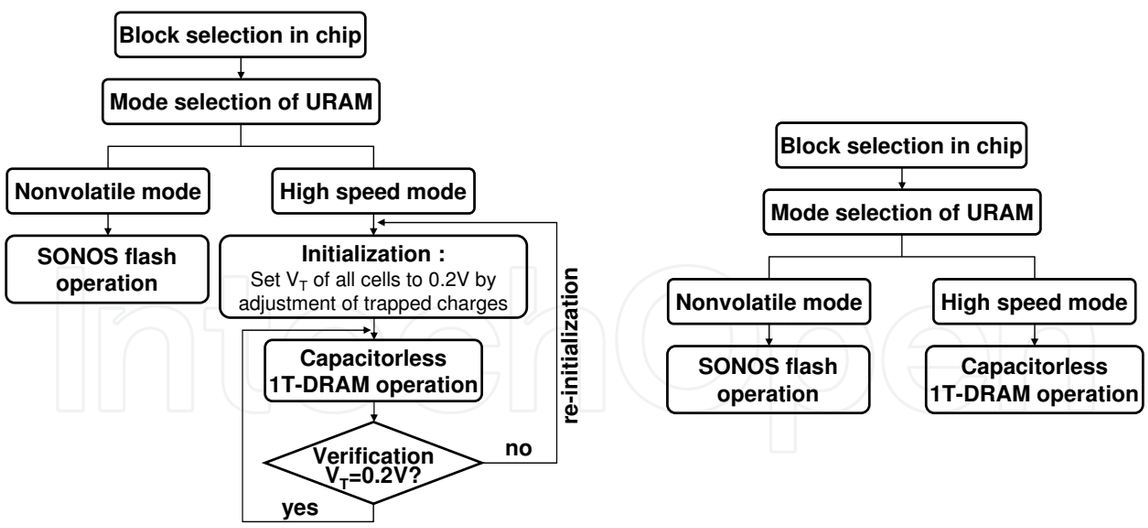


Fig. 5-8. Threshold voltage and sensing current window versus the operation cycles. The threshold voltage shift and sensing current window degradation are found to be negligible, which guarantees very stable URAM operation without soft-programming.



(a) (b)

Fig. 5-9. Operational sequence for URAM. (a) The conventional read method and (b) the parasitic BJT read method. In the conventional read method, the verification and re-initialization loop is necessary due to the soft-program issue. In contrast, the parasitic read method excludes the redundant loop because the interference between the two modes is eliminated.

6. Conclusions

In this chapter, as we confront challenges of current memory technology and as the design rule deviates from the historical scaling paradigm, a novel memory scheme is proposed to continue the roadmap beyond the end point of silicon based memory. Over the scaling to multi-bit era, the multi-functional paradigm is proposed. Whereas the conventional fusion memory pursues high-cost multi-chip-package technology, multi-function is realized in a single memory transistor. The functions of nonvolatile Flash memory and high-speed DRAM are co-integrated, and this memory is named Unified-RAM or URAM. The combination of oxide/nitride/oxide gate dielectric and the floating body structure provide two functions in a single memory cell. In addition, the inherent operational bias domain for two functions allows independent function depending on the end user's demand. The various floating body substrates designed with consideration of the quantum mechanics were proposed in order to confine the excess hole to operate the capacitorless 1T-DRAM. In addition to the conventional silicon on insulator (SOI) substrate, three bulk type floating body substrates were developed. The silicon on n-well (SONW) formed by the deep ion implantation and the silicon on $Si_{1-y}C_y$ (SOSC) formed by epitaxial growth were presented for the potential barrier type approach. Furthermore, the silicon on $Si_{1-x}Ge_x$ (SOSG) was developed for the potential well type substrate. Even though the performance of bulk might be inferior to that of SOI, the bulk can be still useful in terms of cost-effective manufacturing and heat dissipation with a moderate sensing window. After the soft-program issue was certificated, the parasitic bipolar junction transistor (BJT) read method was newly proposed for powerful performance with soft-programming immunity.

As URAM is implemented by using standard semiconductor design and fabrication facility, new products can be manufactured quickly, reducing development time and investment cost. The beauty of URAM lies in the fact that it does not require exotic semiconductor materials, oddly structured parts, exploratory insulator, or an extra photolithography step. URAM is considered to be the next generation for advanced memory technology, which will open a new paradigm shift, and it will be a viable successor to the future embedded memory.

7. References

Brown, W. D. & Brewer, J. E. (1998). *Nonvolatile semiconductor memory technology*, IEEE Press, ISBN-13:978-0780311732, Piscataway, NJ

Chen, C.-E. D. et. al. (1988). Single-transistor latch in SOI MOSFET's, *IEEE Electron Device Lett.*, Vol. 9, No. 12, pp. 636-638, IEEE, ISSN:0741-3106

Gautier, J. et. al. (1997). SOI Floating-Body, Device And Circuit Issues, *IEEE IEDM Tech. Dig.* pp. 407-410, IEEE, ISBN:978-1-4244-237-4

Han, J.-W. et. al. (2007). A Unified-RAM (URAM) Cell for Multi-Functioning Capacitorless DRAM and NVM, *IEEE IEDM Tech. Dig.* pp. 929-932, IEEE, ISBN:978-1-4244-237-4

Han, J.-W. et. al. (2008a). Band offset FinFET-based URAM (Unified-RAM) built on SiC for multi-functioning NVM and capacitorless 1T-DRAM, *IEEE VLSI Symp. Tech. Dig.*, pp. 200-201, IEEE, ISBN:4-900784-00-1

Han, J.-W. et. al. (2008b). Energy Band Engineered Unified-RAM (URAM) for Multi-Functioning 1T-DRAM and NVM, *IEEE IEDM Tech. Dig.* pp. 227-230, IEEE, ISBN:978-1-4244-237-4

Han, J.-W. et. al. (2009a). Gate-to-Source/Drain Nonoverlap Device for Soft-Program Immune Unified RAM (URAM), *IEEE Electron Device Lett.*, Vol. 30, No. 5, pp. 544-546, IEEE, ISSN:0741-3106

Han, J.-W. et. al. (2009b). Gate-Induced Drain-Leakage (GIDL) Programming Method for Soft-Programming-Free Operation in Unified RAM (URAM), *IEEE Electron Device Lett.*, Vol. 30, No. 2, pp. 189-191, IEEE, ISSN:0741-3106

Kim, M. & Osten, H. J. (1997). X-ray photoelectron spectroscopic evaluation of valence band offsets for strained $Si_{1-x}Ge_x$, $Si_{1-y}C_y$, and $Si_{1-x-y}Ge_xC_y$ on Si(001), *Appl. Phys. Lett.*, Vol. 70, No. 20, pp. 2702-2704, AIP, ISSN:1077-3118

Lindert, N. et. al. (1996). Comparison of GIDL in P+-poly PMOS and n+-poly PMOS devices, *IEEE Electron Device Lett.*, Vol. 9, No. 12, pp. 636-638, IEEE, ISSN:0741-3106

Moore, G. E. (1965). Cramming more components onto integrated circuits, *Electronics*, Vol. 38, No. 8, pp. 114-117

Ma, M.-W. et. al. (2007). Impact of High-*k* Offset Spacer in 65-nm Node SOI Devices, *IEEE Electron Device Lett.*, Vol. 28, No. 3, pp. 238-241, IEEE, ISSN:0741-3106

Ni, W.-X. & Hansson, G. V. (1990). Band offset in pseudomorphically grown $Si/Si_{1-x}Ge_x$ heterostructure studied with core-level x-ray photoelectron spectroscopy, *Phys. Rev. B*, Vol. 42, No. 5, pp. 42-50, APS, ISSN:0163-1829

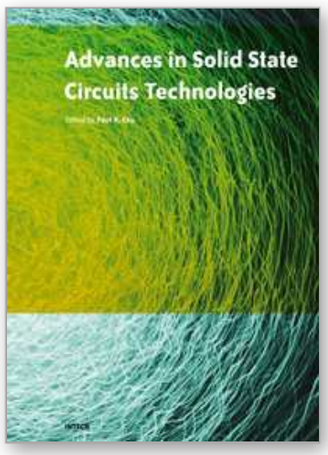
Okhonin, S. et. al. (2007). New Generation of Z-RAM, *IEEE IEDM Tech. Dig.* pp. 929-932, IEEE, ISBN:978-1-4244-237-4

Okhonin, S. et. al. (2001). A capacitor-less SOI 1T-DRAM concept, *IEEE Int. SOI Conf.* pp. 153-154, IEEE, ISBN:0-7803-7439-8

Ranica, R. et. al. (2005). Scaled 1T-Bulk devices built with CMOS 90 nm technology for low-cost eDRAM applications, *IEEE VLSI Symp. Tech. Dig.*, pp. 38–39, IEEE, ISBN:4-900784-00-1

Song, K.-W. et. al. (2008). 55 nm Capacitor-less 1T DRAM Cell Transistor with Non-Overlap Structure, *IEEE IEDM Tech. Dig.* pp. 727-780, IEEE, ISBN:978-1-4244-237-4

IntechOpen



Advances in Solid State Circuit Technologies

Edited by Paul K Chu

ISBN 978-953-307-086-5

Hard cover, 446 pages

Publisher InTech

Published online 01, April, 2010

Published in print edition April, 2010

This book brings together contributions from experts in the fields to describe the current status of important topics in solid-state circuit technologies. It consists of 20 chapters which are grouped under the following categories: general information, circuits and devices, materials, and characterization techniques. These chapters have been written by renowned experts in the respective fields making this book valuable to the integrated circuits and materials science communities. It is intended for a diverse readership including electrical engineers and material scientists in the industry and academic institutions. Readers will be able to familiarize themselves with the latest technologies in the various fields.

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

Yang-Kyu Choi and Jin-Woo Han (2010). Evolutionary Memory: Unified Random Access Memory (URAM), Advances in Solid State Circuit Technologies, Paul K Chu (Ed.), ISBN: 978-953-307-086-5, InTech, Available from: http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/evolutionary-memory-unified-random-access-memory-uram-

INTECH
open science | open minds

InTech Europe
University Campus STeP Ri
Slavka Krautzeka 83/A
51000 Rijeka, Croatia
Phone: +385 (51) 770 447
Fax: +385 (51) 686 166
www.intechopen.com

InTech China
Unit 405, Office Block, Hotel Equatorial Shanghai
No.65, Yan An Road (West), Shanghai, 200040, China
中国上海市延安西路65号上海国际贵都大饭店办公楼405单元
Phone: +86-21-62489820
Fax: +86-21-62489821

© 2010 The Author(s). Licensee IntechOpen. This chapter is distributed under the terms of the Creative Commons Attribution-NonCommercial-ShareAlike-3.0 License, which permits use, distribution and reproduction for non-commercial purposes, provided the original is properly cited and derivative works building on this content are distributed under the same license.

IntechOpen

IntechOpen