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Wireless Communications at 60 GHz: A Single-Chip Solution on CMOS Technology

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1. Introduction

Consumers continuously desire improved connectivity of their electronic devices and the ability for wireless high-definition multimedia streaming, high-speed wireless file transfer, and gigabit wireless local area networks. Currently, the data rates of wireless systems utilizing the unlicensed spectrum such as Bluetooth and the IEEE 802.11 family, cannot deliver multiple-gigabit-per-second data rates due to the small bandwidth allocation. Fortunately, a 7 GHz of spectrum has been made available for unlicensed wireless communications in the 60-GHz band, from 57 to 64GHz in the USA and Canada and from 59 to 66GHz in Japan (Guo et al., 2007) to address this demand.

Ultimately for electronic devices, economic considerations decide the technology used in implementation. Systems are required to be small, low-power and low-cost. To achieve a low-cost solution, a semiconductor technology with high integration capability is needed for implementing these systems. CMOS is a standard and cost-effective process for building digital circuits. Recent advances in millimeter-wave electronics have brought a significant portion of a 60-GHz wireless system to be integrated onto a single CMOS chip. Unfortunately, compared to other more expensive processes that are capable of millimeter-wave circuit design such as SiGe and GaAs, CMOS has greater process variability, lower carrier mobility constants, and smaller device breakdown voltages. This makes 60-GHz wireless transceiver design and implementation on CMOS particularly challenging.

In this chapter, we discuss the development of a 60-GHz wireless transceiver-on-a-chip on a 130-nm CMOS technology. The challenges and solutions for the design of 60-GHz components on CMOS including radio-frequency (RF) bandpass filter (BPF), power amplifier (PA), low-noise amplifier (LNA), mixers, voltage control oscillator (VCO) are described. These components are utilized to build the world's first all-integrated 60GHz wireless transceiver on CMOS which is also presented in this chapter. The transceiver also includes a digital control interface (DCI). Experimental results are provided.

2. System architecture

In this section we outline the system architecture of the designed 60-GHz single-chip wireless transceiver. This all-integrated transceiver comprises a transmitter, a receiver, and a phase-locked loop (PLL) as shown in Fig. 1. The transmitter/receiver front-end is implemented as a homodyne architecture. The digital control interface included on the chip allows dynamical tuning of the biasing conditions of the transceiver for optimum performance.

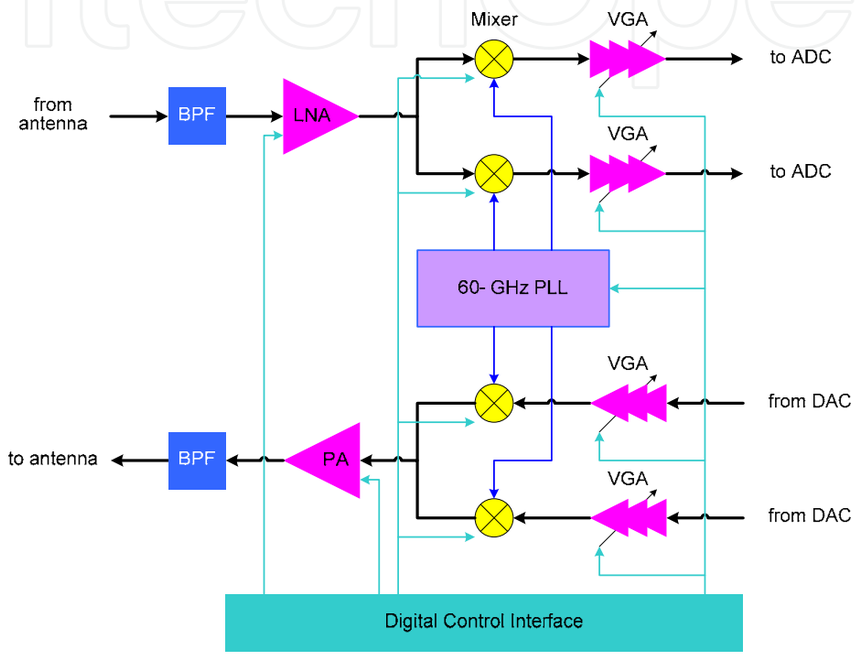


Fig. 1. Block diagram of the 60-GHz wireless transceiver

In the receiver an integrated passive BPF is employed to reject out-of-band interference to improve the receive sensitivity. The LNA amplifies the input signal while contributing a minimal amount of noise. Following the LNA are two mixers that perform frequency conversion for inphase/quadrature (I/Q) channels. These mixers are double balanced Gilbert cell mixer which offers high isolation from its local oscillator (LO) port to its RF port which is critical for homodyne transceivers (Abidi, 1995). Two variable gain amplifiers (VGAs) following the mixers have built-in DC offset cancellation loop to suppress the DC offset caused by self-mixing effect in the mixer. For the transmitter, the high-power amplifier is integrated on-chip and is optimized to drive an off-chip 50Ω-impedance transmit antenna. The BPF between the PA and the transmit antenna minimizes out of band emission in the transmitter. The local oscillation signals required for the operation of the mixers in the transmitter and receiver are provided by a PLL system. At the center of the PLL is a VCO based on a push-pull architecture. This VCO has a tuning range from 57 to 64GHz.
In the following sections, details about the design and performance of each building block of the single-chip 60-GHz transceiver on CMOS are presented.

3. Integrated passive RF filter

RF filters play an important role in radio transmitters and receivers where these filters suppress out-of-band signals generated by high-power amplifiers in the former and reject interferers to improve the sensitivity of the later. It is strongly desired to have these filters integrated on the same chip with the transceiver to reduce the overall cost and form factor of the radio. One of the biggest challenges that hinder designers from integrating RF filters on CMOS is the lossy silicon substrate. The high resistive loss induced in the silicon substrate due to electrical coupling deteriorates the quality factor of resonators implemented on CMOS which leads to higher insertion loss of filters based on these resonators (Yang et al., 2008).

The analysis and design of passive RF filter on CMOS is a challenging task due to the thick metal layers and the thin, multi-layer dielectric material on CMOS. For a thick metal trace the current distribution and the voltage potential (or E- and H-field distributions) along the top surface and those along the bottom surface are not identical. Meanwhile, the fringing coupling due to the sidewalls of the metal traces becomes significant when the metal traces grow thicker. These effects render the conventional design method which assumes thin-film metal trace on thick substrate inaccurate. In the past, where the thin-film and homogeneous, thick substrate conditions applied, theoretical and empirical design equations combined with 2D or 2.5D electromagnetic simulators are sufficient for the analysis and design of RF filters. For the thick-film, thin-substrate case of CMOS, a more rigorous approach must be taken to accurately design the filter.

In this section, the design of millimter-wave RF band-pass filters (BPFs) on CMOS technology will be presented. Along with a design methodology, methods to counter the deteriorate effects such as signal loss and coupling in millimetre-wave filters will be introduced to facilitate the realization of these filters on a CMOS technology. A BPF working on the 57-66GHz band with a compact size, a low insertion loss, and a good out-of-band rejection has been successfully implemented on the IBM 130nm CMOS technology using these techniques.

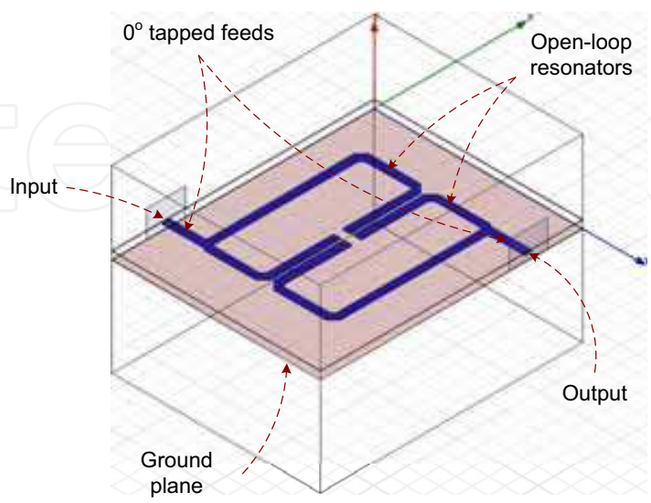


Fig. 2. HFSS model of the 60-GHz two-pole second-order open-loop resonator BPF

The designed BPF is a second-order filter based on coupled open-loop resonators. The open-loop resonators are built from half-wavelength microstrip lines. Compared to the other planar waveguide available on integrated circuit technology, the coplanar waveguide, microstrip line can be made more compact. The microstrip line also has a ground plane that shields the electro-magnetic field from coupling to the lossy silicon substrate. The microstrip structure, therefore, completely solves the problem of signal loss in the silicon substrate. The structure of the BPF as illustrated in Fig. 2 shows two rectangular resonators laid out side-by-side for electromagnetic coupling purpose. Two 0° tapped feeding structures are added to the input and output of the filter to create transmission zeros in the stopband of the filter (Lee & Tsai, 2000). These transmission zeros improve the stopband rejection of the filter. The positions at which the tapped feeding lines are connected to the resonators are optimized to ensure low ripple and low insertion loss in the passband.

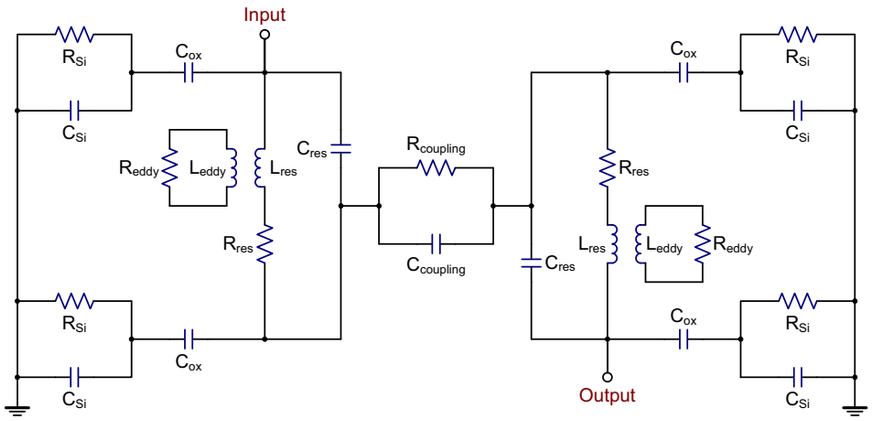


Fig. 3. A model of electromagnetic coupling between adjacent resonators on CMOS

The operation and performance of the BPF can be analyzed by investigating a lumped model of the filter. Fig. 3 illustrates the major coupling components in the two resonators of the BPF described in Fig. 2. C_{si}, and R_{si} are the capacitance and resistance, respectively, of the silicon substrate underneath the resonator. C_{ox}, is the capacitance between the metal trace of the resonator and the ground plane. C_{res} and L_{res} are the effective capacitance and inductance of the resonators. R_{res} accounts for the metal conductive loss in strips due to metal's intrinsic resistive characteristics and the skin effect that cannot be neglected at high frequencies. $C_{coupling}$ represents the proximity coupling that governs the transfer function of the filter. $R_{coupling}$ accounts for the coupling loss between two resonators. R_{eddy} represents the loss due to the eddy currents induced in the resistive substrate. The design process determines the size of the resonators and the space between them so that the desired transfer function is obtained.

The designed filter is fabricated on the IBM 130nm CMOS technology and its microphotograph is shown in Fig. 4. In order to minimize the unwanted coupling through the substrate and to reduce the induced eddy currents, the substrate was segmented into regions of high impedance. This is accomplished by implementing a high impedance substrate material between the substrate under each resonator. A high impedance bounding box is also built around the whole BPF structure. To satisfy the metal density requirements of the CMOS process, floating metal arrays are added to the layout as can be seen in Fig. 4.

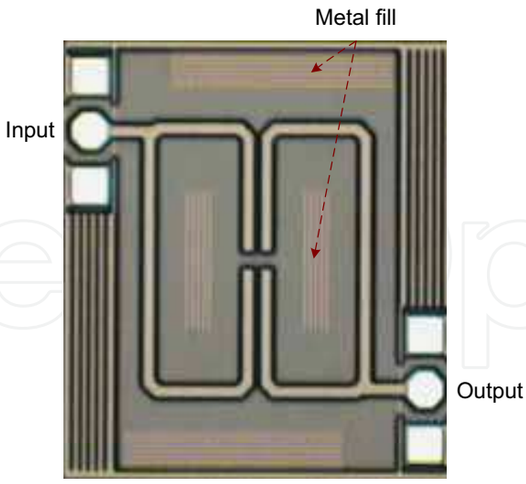


Fig. 4. Micrograph of the 60-GHz two-pole second-order open-loop resonator BPF. The footprint (excluding the testing pads) is 415μm × 503μm.

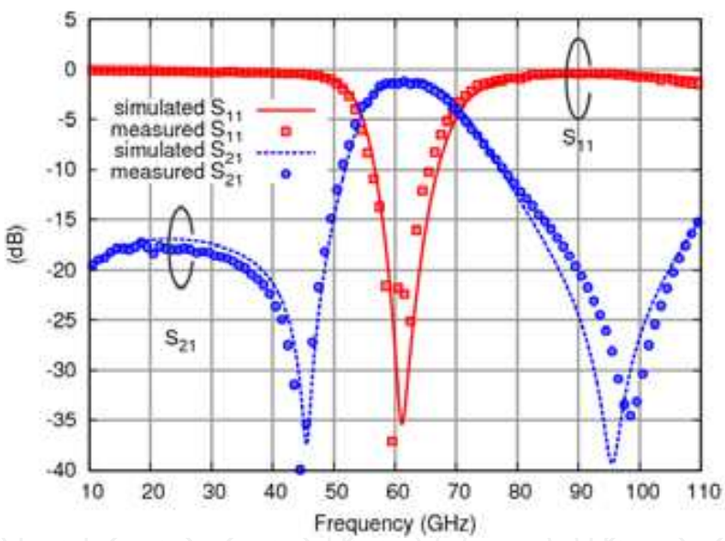


Fig. 5. Insertion loss and return loss of the 60-GHz two-pole second-order open-loop resonator BPF

HFSS, a state-of-the-art 3D full-wave electromagnetic simulator from Ansoft, Inc., is utilized to accurately estimate the performance of the BPF. Simulation and measurement results for the designed filter are shown in Fig. 5. A good match between simulation results and measurement results is achieved. The filter has a 1-dB pass-band from 57GHz to 66GHz as expected. The insertion loss is 1.5dB at mid-band frequency. The return loss is less than 9.2dB across the whole pass-band. Two transmission zeros, located at 45GHz and 98GHz, introduced by 0° tapped feed structure provide a steep roll-off in the stop-band. The side lobe in the lower stop-band is better than -18dB. This BPF has also been integrated in the 60-GHz CMOS wireless transceiver designed in this work. To the authors' knowledge, this is the first CMOS RF BPF fully integrated with a 60 GHz transceiver.

4. Low-noise amplifier

Millimeter-wave LNA design has long been dominated by compound semiconductor technologies such as GaAs and InP which have superior gain and noise performance. Only recently have silicon based technologies such as SiGe BiCMOS and CMOS, which are much cheaper than compound semiconductor technologies, advanced to a level that is capable of millimeter-wave operation. The design in (Doan et al., 2005) is the first 60-GHz amplifier on CMOS and is more a general purpose amplifier than a low-noise amplifier. The 90-nm CMOS LNA presented in (Yao et al., 2006) has a peak gain of 14.6dB at 58GHz and a minimum noise figure (NF) of 5.5dB. In general, these LNA designs are capable of providing gain for a portion of the 60-GHz band but not the entire spectrum from 57 to 66GHz, which covers all 60-GHz bands in USA, EU, and Japan, because their gain is low at the edge of the frequency band. For example, the gain of the LNA in (Yao et al., 2006) reduces to 8dB at 64GHz. Also, the NFs of these LNA are much higher at the edges of the band compared to that at the center frequency. Recent reported LNA designed on 90-nm CMOS technology (Cohen et al., 2008) achieves a very low NF of only 4.4dB. On 65-nm CMOS technology, 60-GHz LNA design was also reported to have a NF of 5.9dB and a variable gain ranging from 5dB to 15dB (Natarajan et al., 2008).

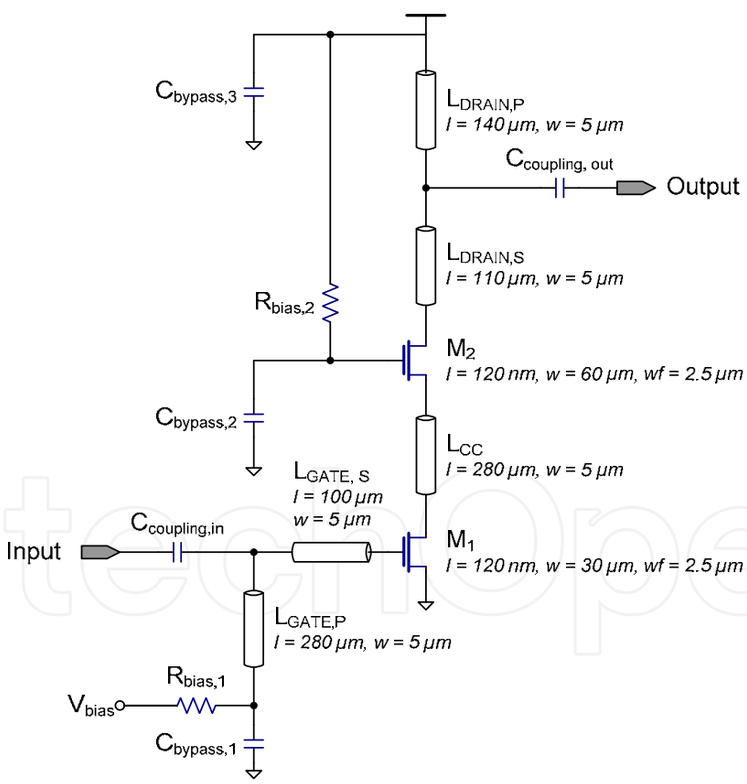


Fig. 6. Schematic of the modified cascode amplifier with intra-stage inductor

In this section the design of a 60-GHz LNA on a 130-nm CMOS process will be discussed. This LNA differs from published CMOS LNA designs in that it can operate across the entire 60-GHz band from 57 to 66GHz with less variation in gain and noise figure. The LNA which

includes four modified cascode stages was implemented and fabricated as part of the 60-GHz transceiver. Simulation results will be presented.

Millimeter-wave frequency MOSFETs are laid out as multi-finger device. Determining the right configuration of the transistor, including its gate length, gate width, and finger width, and the right biasing condition for the transistor is the crucial step to achieve the best performance of the transistor (Doan et al., 2005). For this particular CMOS technology, the optimum transistor configuration and biasing condition taken into account its gain, noise, and power consumption performance have been determined by simulation. A 130-nm gate length, 30-μm gate width, 2.5-μm finger width transistor biased at a drain current of 6mA is selected as the input transistor (M_1) of each cascode gain stage shown in Fig. 6. A major modification made to the conventional cascode stage is the adding of an intra-stage inductor L_{CC} between the input transistor M_1 and the cascode transistor M_2. This inductor helps reduce the noise figure without significantly reducing the gain of the cascode stage.

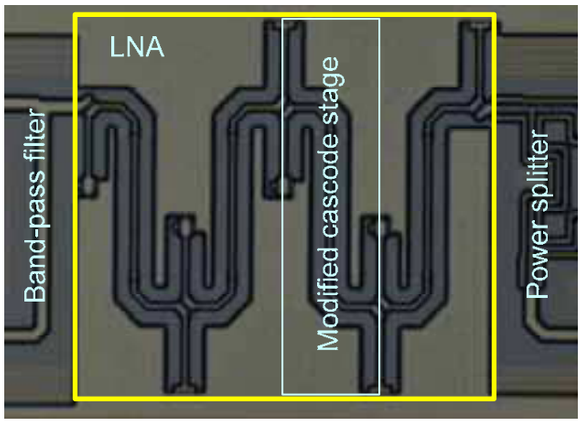


Fig. 7. Microphotograph of the four-stage LNA integrated in the 60-GHz receiver

An LNA was realized by cascading four modified cascode stages. A microphotograph of the LNA is shown in Fig. 7 as part of the receiver. Since the LNA was not taped out separately, its performance cannot be characterized experimentally. An extracted view of the LNA layout including the critical parasitic resistance and capacitance was used for the simulation of the performance of the LNA.

The performance of the LNA in the frequency band from 57GHz to 66GHz is shown in Fig. 8 (a)–(c). The maximum small-signal power gain, S_{21}, of the LNA is 17.1dB at 58GHz. From 57GHz to 65GHz, the gain of the LNA is above 14dB. The 3-dB bandwidth of the LNA is therefore 8GHz. At 66GHz, the gain is reduced to 13.1dB. The noise figure of the LNA varies from 7.2dB to 7.7dB. The input and output of the LNA match well to 50Ω with return losses, S_{11} and S_{22}, less than -12dB across the whole band. The reverse isolation, $-S_{12}$, is more than 80dB. The input third-order inter-modulation product, IIP_3, of the LNA was simulated to be 7.2dBm.

The performance of the LNA designed in this work is summarized in Table 1 along with the performance of previously published 60-GHz CMOS LNAs. These LNAs are compared by using the widely accepted Figure of Merit (FoM) defined in the International Technology Roadmap for Semiconductors (ITRS, 2007). Compared to other published CMOS LNAs

designed on 130-nm CMOS technology (Doan et al., 2005; Lo et al., 2006) the LNA in this work has higher FoM. The noise figure in this design also exhibits less variation. The comparison shows a distinct advantage of technology scaling in LNA design in which the LNAs designed in later technology, for example the 90-nm technology as reported in (Yao et al., 2007), have much higher FoM than those designed in 130-nm technology.

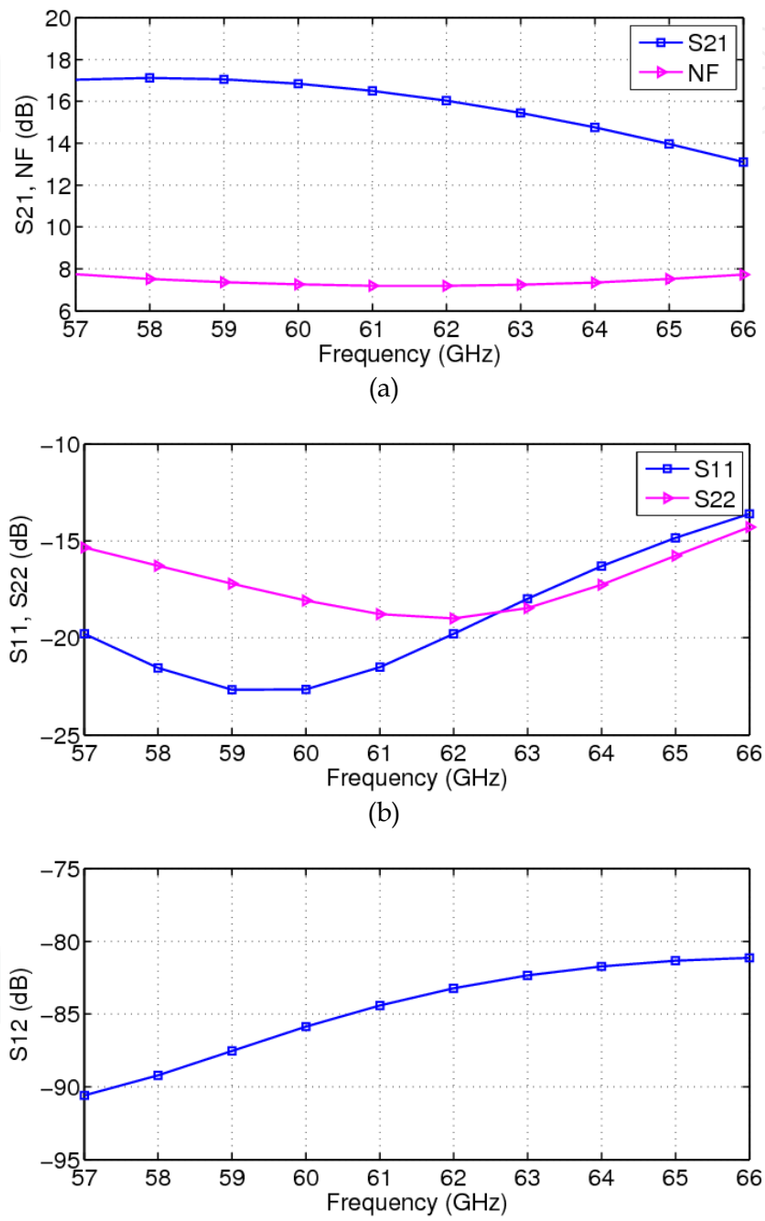


Fig. 8. Simulated performance of the LNA: (a) gain and noise figure, (b) input and output return losses, and (c) reverse isolation

Reference	CMOS tech.	Freq. (GHz)	VDD (V)	P_{DC} (mW)	NF (dB)	Gain (dB)	IIP_3 (dBm)	FoM
(Doan et al. 2005)	130-nm	51-65	1.5	54	8.8-9.7	10.4-11.9	-0.5	2.1
(Lo et al. 2006)	130-nm	51-58	2.4	72	7.1-9.5	20-24.5	-12	3.5
(Heydari et al. 2007)	90-nm	60	1.0	10.5	6.0	12.2	(n.a.)	
(Yao et al. 2007)	90-nm	58	1.5	24	4.5	14.6	-6.8	8.1
This work	*130-nm*	*57-66*	*1.5*	*36*	*7.2-7.7*	*13.1-17.1*	*-7.2*	*3.8*

Table 1. Performance comparison of the LNA in this work and previous published 60-GHz LNAs on CMOS technology

5. Power amplifier

A PA is used to amplify and efficiently deliver an RF signal it to a load which, in this design, is the transmitting antenna. At millimetre-wave frequencies the design of PAs on CMOS is challenging as the operating frequencies are a significant portion of the transistor maximum frequency of oscillation (f_{max}), thus the designer has a reduced gain available for use. As CMOS scales toward smaller feature size the breakdown voltage of the active device also reduces. This significantly limits the output power of the amplifier. The power amplifier needs to be optimised to smaller load impedances, higher current and larger device sizes to achieve a sufficient output power. Currently very few millimetre-wave power amplifiers have been published (Yao et al., 2006; Wicks et al., 2007). In addition, many implementations of high data rate systems are based on an orthogonal frequency division multiplexing (OFDM). OFDM signals are characterised by a high peak to average ratio (PAR) and require low distortion in order to minimise inter carrier interference. In order to contend with a high PAR the Doherty PA is a good architectural candidate.

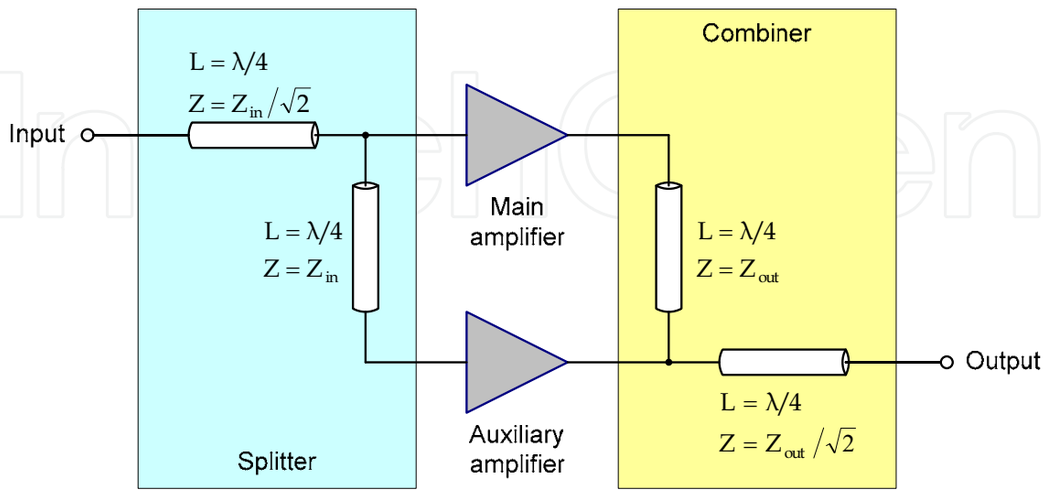


Fig. 9. Doherty power amplifier architecture

The Doherty PA employs multiple amplifiers, each contributing amplification for only a subset of the power rage and is used to boost both the power added efficiency (PAE) at low power and the 1-dB compression power (P_{1dB}) and saturation power (P_{sat}). The Doherty amplifier shown in Fig. 9 employs two amplifier cells, the main amplifier cell and the auxiliary amplifier cell. A transmission line network is used to split the input signal into two amplifiers and comprises a quarter wavelength transmission line connecting the input to the main amplifier cell with characteristic impedance of $Z_0 = 50\Omega$, and a quarter wavelength transmission line with characteristic impedance of $Z_0 = 50/\sqrt{2}\ \Omega$ connecting the inputs of the main amplifier cell with the auxiliary amplifier cell. An identical transmission line network is used to combine the outputs of the two amplifiers, with the output transmission line connection used to compensate for the phase shift of the splitter. Both the input and output networks are matched to 50Ω impedance.

The size of the transistors used in each main/auxiliary amplifier need to be carefully investigated. Each transistor device needs to be carefully laid out to minimise parasitic capacitance and substrate resistance. In this design each amplifier consists of five cascode stages. The cascode unit building block was used in order to increase gain of the PA by reducing the Miller capacitance, and also to improve the amplifiers stability. When biased at 200μA/μm each cascode stage possesses a maximum available gain (MAG) of 7dB at 60GHz. Micro-strip waveguides were used for impedance matching, interconnects and for biasing of each amplifying stage. These cascode stages are AC coupled to allow independent basing of the transistors for optimum operating conditions.

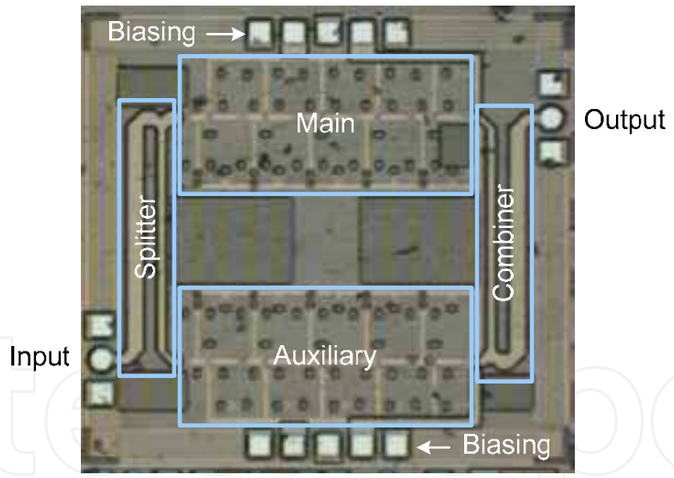


Fig. 10. Microphotograph of the 60-GHz Doherty power amplifier. The size of the PA including testing pads is 1410μm by 1310μm.

The power amplifier is fabricated on the IBM 130-nm CMOS technology and its microphotograph is shown in Fig. 10. The measured S-parameters shown in Fig. 11 reveal a peak power gain, S_{21}, of 15dB and a 3-dB bandwidth of 6GHz from 56.5GHz to 62.5GHz. The input and output return losses, S_{11} and S_{22}, are less than -10dB for the entire frequency band of interest from 57 to 66GHz. The output 1-dB compression power, P1dB, which can be derived from the high-power performance of the PA shown in Fig. 12, is 7dBm. Fig. 13 shows the current consumption in the main and auxiliary amplifier at different input power

levels. The power added efficiency (PAE) of the PA is maximized when both the main and auxiliary amplifiers are equally powered. The maximum PAE for this PA is 3%.

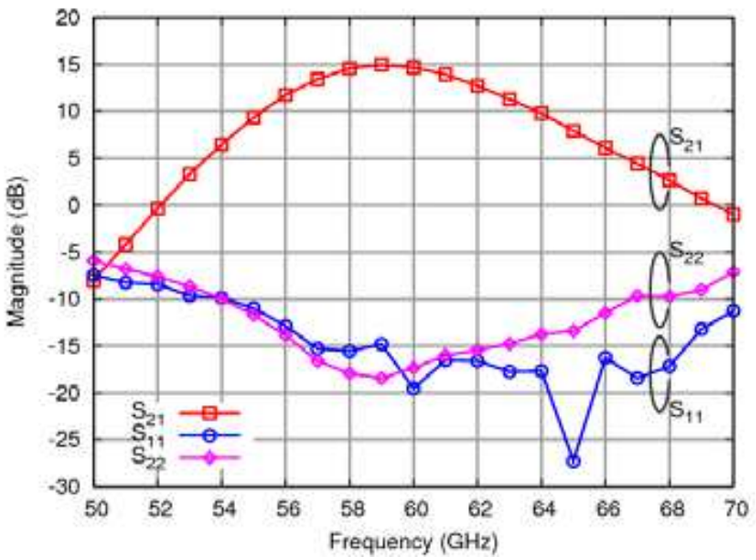


Fig. 11. Measured small-signal performance of the 60-GHz Doherty power amplifier

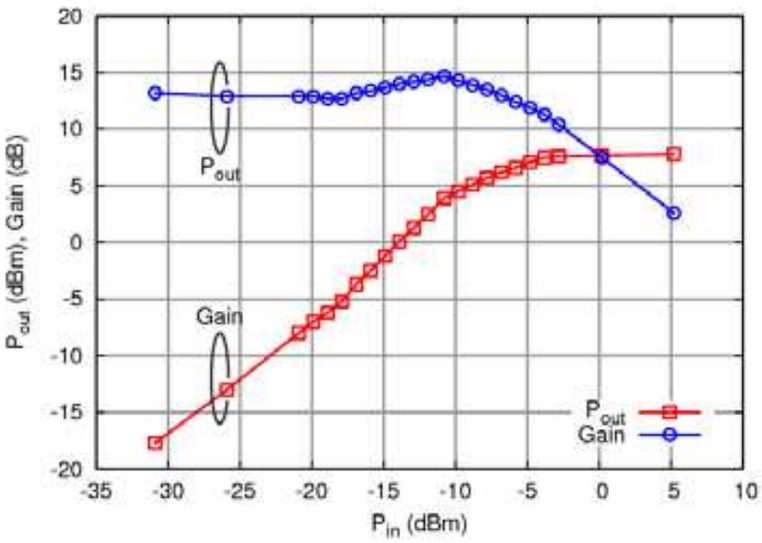


Fig. 12. Measured output power and gain of the 60-GHz Doherty power amplifier

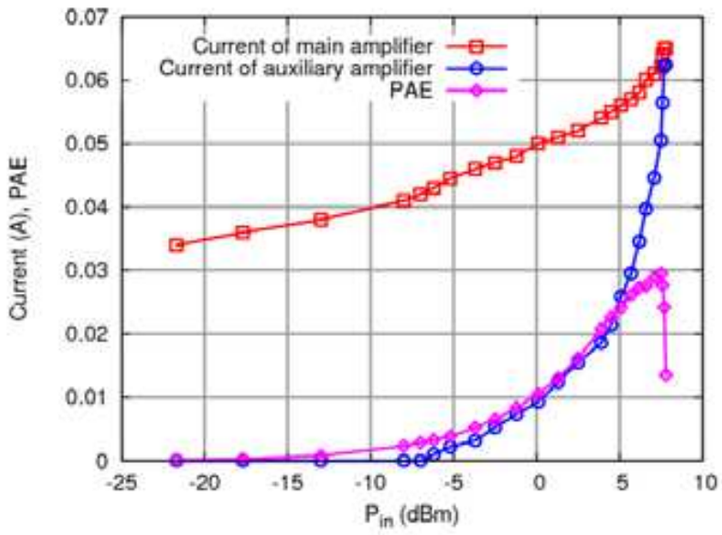


Fig. 13. Measured current consumption and power added efficiency of the Doherty PA

The International Technology Roadmap for Semiconductors (ITRS, 2007) has defined an FoM for the PA which links the output power (P_{1dB}) with the gain, PAE, and frequency as a standard to compare different PAs. Table 2 provides a comparison of this PA with other published CMOS millimeter-wave PAs in terms of this FoM.

Reference	CMOS tech.	Freq. (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	PAE (%)	Architecture	FoM
(Yao et al. 2007)	90-nm	60	5.2	9.3	6.4	7.4	3-stage cascode	7.5
(Suzuki et al. 2008)	90-nm	60	8.0	10.6	8.2	-	3-stage common source	-
	90-nm	77	9.0	6.3	4.7	-		-
(Chowdhury et al. 2008)	90-nm	60	5.6	12.3	9.0	8.8	3-stage transformer	19.5
(Wicks et al. 2008)	130-nm	77	6.0	8.1	6.3	0.5	5-stage cascode	2.1
This work	*130-nm*	*60*	*13.5*	*7.8*	*7.0*	*3.0*	*Doherty*	*15.2*

Table 2. Performance comparison of the PA in this work and published millimetre-wave PAs on CMOS technology

6. Mixer

The down-conversion mixer in the receiver is used to translate the input signal from RF to an intermediate frequency (IF) for processing by baseband circuits. An important consideration in homodyne receiver structures is the LO-to-RF isolation of the mixer. LO self-mixing (Lee, 2004), occurs when the LO signal (which is at the same frequency as the RF signal) leaks to the input of the mixer and then mixes with itself, produces a time varying DC offset which significantly degrades the receiver's performance especially in OFDM systems. In the literature, few results have been presented for CMOS mixers which are

suitable for homodyne architectures operating at the 60-GHz band (Emami et al., 2005). In this section we describe the design of a 60-GHz double balanced Gilbert cell mixer with high LO-to-RF isolation on CMOS technology.

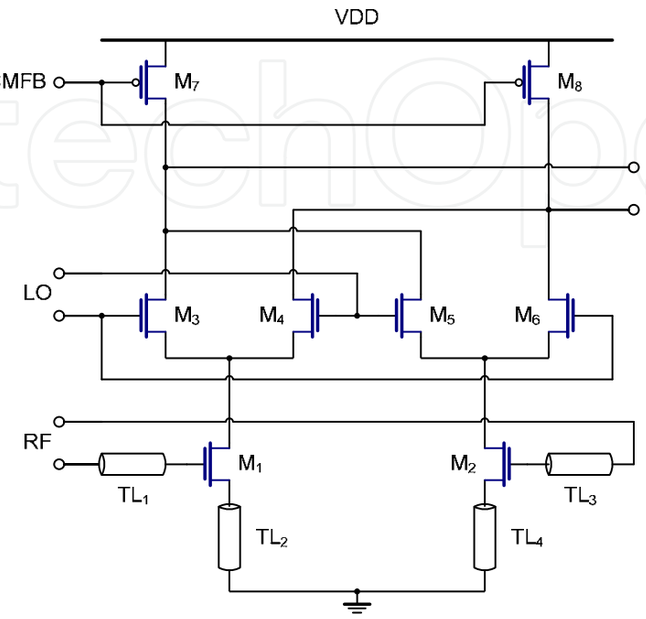


Fig. 14. Double-balanced Gilbert cell mixer

Fig. 14 shows the schematic of the double-balanced mixer where biasing circuits have been omitted for clarity. TL_2 and TL_4 are two microstrip lines serving as source degeneration inductors and TL_1 and TL_3 are used to match the RF input to 50 Ω. The input impedance looking into the transconductance stage formed by M_1 and M_2 can be shown to be equal to

$$Z_{in} = j\omega L_{TL2} + \frac{1}{j\omega C_{gs}} + \frac{g_m L_{TL2}}{C_{gs}} + j\omega L_{TL1} = j\omega L_{TL2} + \frac{1}{j\omega C_{gs}} + \omega_T L_{TL2} + j\omega L_{TL1}. \quad (1)$$

The expression above shows that by adjusting $TL_{1,2}$ we can match the input impedance to 50Ω for all different sizes of $M_{1,2}$. It also can be shown that the inductive degeneration increases linearity without raising the noise (Terrovitis, 2002). More over, by choosing the optimum number of fingers of $M_{1,2}$, the minimum noise figure, NF_{min}, can also be achieved simultaneously with input port matched.

The loads used in this Gilbert cell mixer as shown in Fig. 14 are a pair of PFET transistors. This type of load is chosen in order to achieve sufficient bandwidth and gain given the limited voltage headroom available when using a 1.2 V power supply. To get a higher output resistance for these transistors, non-minimum channel length has been used and the PFETs are biased in the strong inversion region. However, in order to drive a fixed amount of current, the longer the channel, the wider the width of a transistor is required, which may result in a large size of these PFETs. Thus, a trade-off must be made when determining the size of the PFETs. A source follower buffer, not shown in Fig. 14, is added to the output of the mixer to isolate the mixer core circuit and subsequent stages.

Because of the short wavelength of 60 GHz special considerations must be given to make the circuit as symmetrical as possible in layout to maintain balance and common mode rejection. Transmission line crossings as well as difference in path lengths are avoided when possible since these mismatches increase the imbalance and reduce the isolation between LO, RF, and IF ports. In this design, microstrip lines were used to implement the degeneration impedance, matching networks and critical interconnects that carry high-frequency signal. Micro-strip lines on silicon are typically implemented using the top- layer metal as the signal line, and the bottom-layer metal for the ground plane. The metal layers on which the signal line and the ground plane must be carefully determine so that a simple layout of the mixer can be attained without degrading the quality factor of the microstrip lines.

A 60-GHz double-balanced CMOS mixer with high LO-to-RF isolation was designed and fabricated following the design method described above. A microphotograph of the mixer is shown in Fig. 15. This mixer achieves a voltage conversion gain of better than 2dB, as shown in Fig. 16, input-referred IP3 of −8dBm and LO-to-RF isolation of greater than 36dB, as shown in Fig. 17, when driven with an LO input of 0dBm.

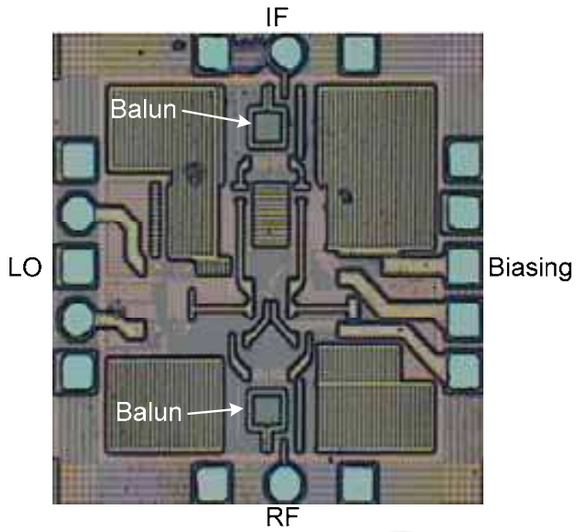


Fig. 15. Microphotograph of the 60-GHz double balance mixer on CMOS with on-chip transformer baluns for testing purpose

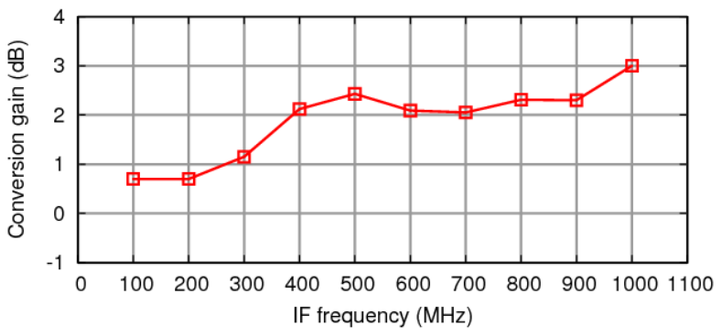


Fig. 16. Conversion gain of the 60-GHz double balance mixer on CMOS

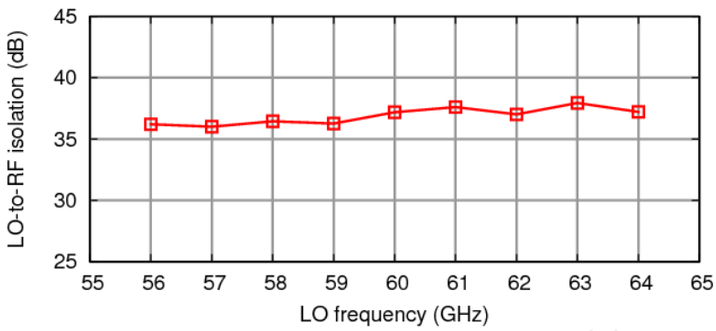


Fig. 17. LO-to-RF isolation of the 60-GHz double balance mixer on CMOS

7. Voltage controlled oscillator

The output power, tuning range and phase noise of the voltage controlled oscillator (VCO) significantly affect the performance of the transceiver. In VCO design the voltage controlled frequency of operation is achieved via voltage dependant capacitance devices such as varactors. In many cases the phase noise of these oscillators is limited by the ability to build high-quality inductors and varactors which form the LC tank that determines the frequency of the VCO. In this application the VCO is required to have: a tuning range of 9 GHz, a phase noise less than -90 dBc/Hz at 1 MHz and a sufficient output power to drive the four mixers as shown in Fig. 1. Such stringent requirements mandate a trade-off between tuning range and phase noise during the design of the VCO.

In MOS technology a varactor can be implemented by shorting the source and the drain terminals of a MOSFET together and applying a control voltage across its gate and source/drain terminals. The bias voltage governs the charge distribution in the channel and subsequently the capacitance the varactor. To achieve maximum possible tuning range with acceptably low phase noise, carefully designed inversion mode MOS varactors are employed. For this particular 130-nm CMOS technology, the length of the NMOS varactors are set equal to 260nm in order to achieve a capacitance tuning ratio of 3. An important consideration in VCO design is the gate leakage current of the varactor increases the VCO's phase noise and its parasitic capacitance reduces the oscillation frequency (Lee & Liu, 2007).

Three candidate architectures for high-frequency VCO are fundamental VCO, VCO with frequency doubler, and push-push VCO. The fundamental architecture is not very efficient in this application since it has narrow tuning range and also requires a wide band divider in the phase locked loop (PLL) which can consume significant power and space. Architectures based on frequency doubling or push-push topology are better choices because they can achieve twice the tuning range of the fundamental architecture. Another advantage of these architectures is that the varactors operate at a lower frequency and have a higher quality factor which results in reduced phase noise. Among these two architectures, the frequency doubling architecture requires additional circuits such as a doubler/multiplier and filters which can consume considerable space and power. Additionally insufficiently filtered harmonics generated by the doubler can modulate the desired output frequency of the VCO and increase the phase noise. The push-push architecture combines frequency generation and frequency doubling in one circuit. In the push-push oscillator the fundamental and odd

harmonics cancel and power is delivered to the load at even harmonics. The push-push architecture is chosen for this application.

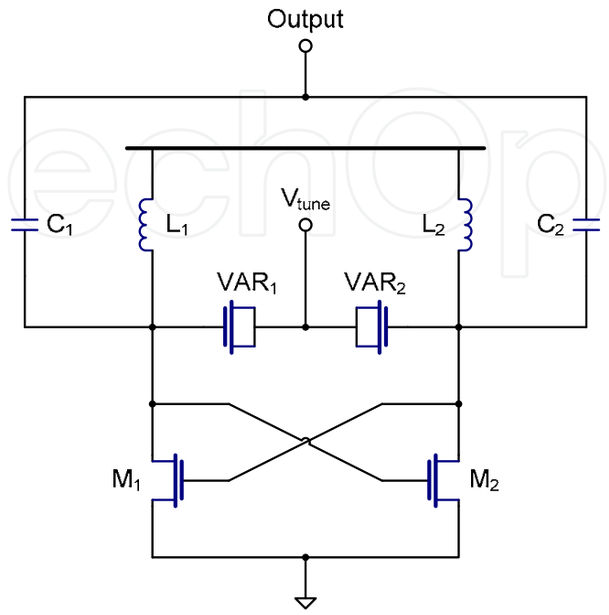


Fig. 18. Circuit diagram of the push-push voltage controlled oscillator

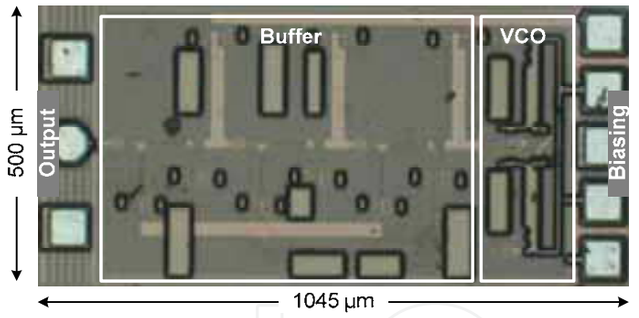


Fig. 19. Microphotograph of the push-push voltage controlled oscillator

The differential cross-coupled LC oscillator with push-push output is shown in Fig. 18. The LC tanks composing the inductor, $L_{1,2}$, and the varactors, $VAR_{1,2}$, determines the frequency of oscillation. Frequency dependent signals at the drain of M_1 (M_2) is cross-coupled to the gate of M_2 (M_1) which creates a negative impedance $-1/g_m$ where g_m is the transconductance of $M_{1,2}$. This negative impedance is sized to exceed the losses of the LC tank to ensure sustained oscillation. Most of designs include a tail current source to set the bias current and provide high impedance which rejects noise from the power supply. However, due to the mixing effect caused by nonlinearity in $M_{1,2}$, the low frequency noise of the tail current source is up converted to the output frequency of the oscillator and degrades the phase noise of the oscillator. In this design, the current source is omitted to suppress this contribution to the phase noise. The circuit shown in Fig. 18 is implemented on standard 130nm CMOS technology. In this design the transistors $M_{1,2}$ have 50 fingers and total width

of 50µm. The NMOS varactors $VAR_{1,2}$ are implemented as a multi-finger structure to reduce gate resistance and enhance the resonator's quality factor. The inductors $L_{1,2}$ are fabricated on the top metal layer to achieve the highest quality factor possible. These inductors are realized as 100µm-long, 25µm-wide RF transmission lines and have an equivalent inductance value of 50pH. A microphotograph of the VCO is shown in Fig. 19.

The fabricated VCO has an output frequency range of 65.8GHz to 73.6GHz as shown in Fig. 20. After calibrating the cable and pads loss, the output power at 70GHz is -4dBm. The core power consumption is 32mW. The phase noise was measured by down converting the VCO's signal to an intermediate frequency of 2.5GHz. The measured phase noise is -92 dBc/Hz at 1 MHz offset (from a center frequency of 66GHz) and -107 dBc/Hz at 10 MHz offset (from a center frequency of 66GHz). Frequency variation with temperature was also measured from 0 to 70 degrees Celsius. The maximum frequency deviation is less than 200MHz in this temperature range as illustrated in Fig. 21.

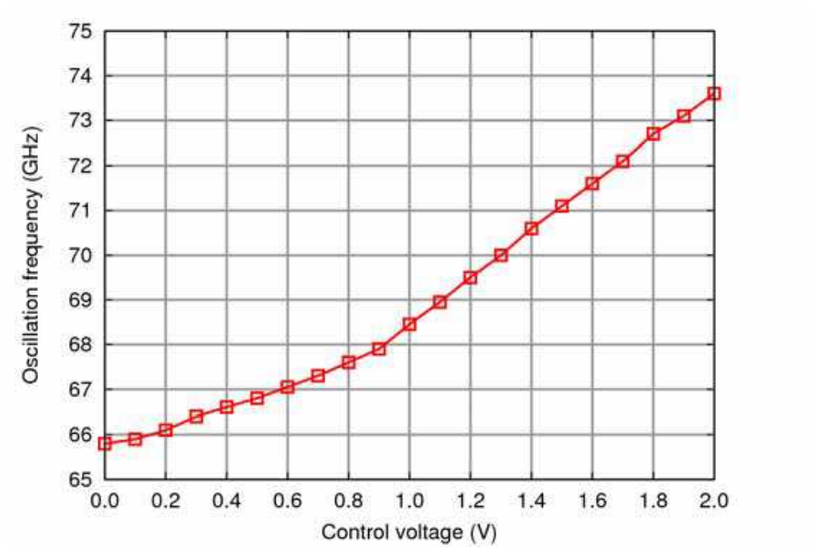


Fig. 20. Output frequency versus control voltage of the VCO

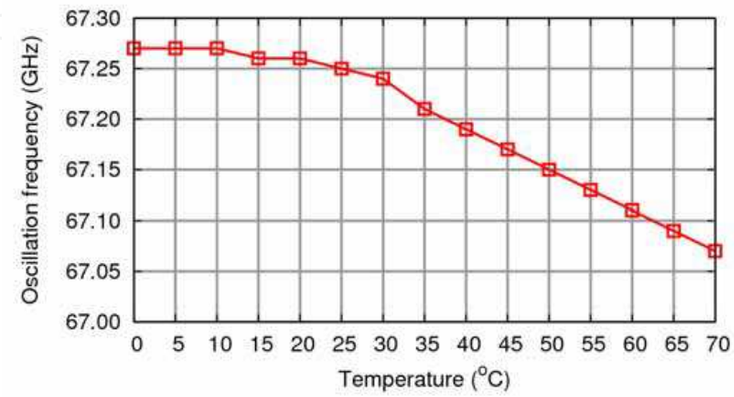


Fig. 21. Frequency shift due to temperature variation

8. Biasing and control

The advancement of CMOS technology is driven by digital integrated circuits which operate faster with transistors with shorter channel length and consume less power with lower power supply voltage. These advantages of digital circuits are due to the fact that digital circuits are less sensitive to temperature, voltage, and power (PVT) variation compared to analog/RF circuits. Analog/RF circuits require special treatment during the design to reduce their sensitive to PVT variation that is significant on CMOS integrated circuits. The 60-GHz transceiver chip designed in this work adopts an on-chip Digital Control Interface (DCI) to digitally tune the behaviour of analog/RF components to remedy the performance degradation due to PVT variation thereby increasing the overall yield of the transceiver.

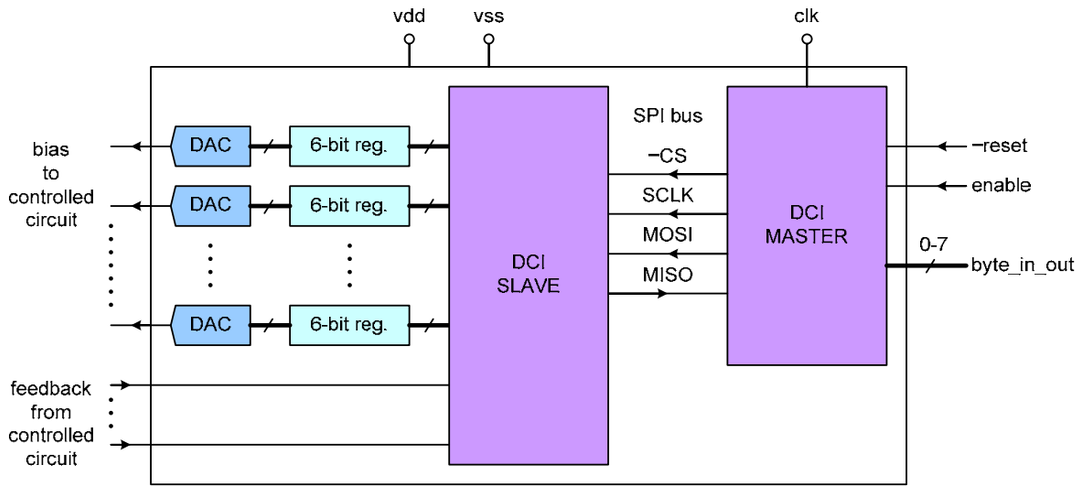


Fig. 22. Block diagram of the digital control interface

The DCI architecture is shown in Fig. 22. It comprises a DCI master and a DCI slave communicating with each other via a serial peripheral interface (SPI) bus and a bank of 6-bit registers and 6-bit digital-to-analog converters (DACs) connected to the DCI slave. For a two-chip radio solution, the DCI master resides on the digital/baseband chip while the DCI slave, register bank, and DAC bank reside on the analog/RF chip.

A tuning algorithm implemented on the digital chip will determine when a certain biasing voltage needs to be changed. The tuning algorithm will then send a request to the DCI master indicating the address of the register and the new value of the register. The DCI master passes these values to the DCI slave, via the SPI bus, which outputs the new value to the required register. The corresponding DAC translates the value stored in the register to the required analog voltage. The DCI slave can also receive feedback from analog/RF circuits and transfer this to the digital chip to assist the tuning algorithm. Real-time monitoring and tuning of the operation of the transceiver is therefore made possible with the integrated DCI.

The layout of the DCI is shown in Fig. 23. In this design, the DCI master and DCI slave are implemented together on the 60-GHz analog/RF chip.

Fig. 23. Layout of the digital control interface

9. 60-GHz single-chip transceiver on CMOS

A 60-GHz single-chip CMOS transceiver was realized by integrating the circuits described above on a single silicon substrate. A microphotograph of the designed chip is shown in Fig. 24. The die measures 5mm by 5mm. Prior to this work, 60-GHz transmitters and receivers have been implemented on CMOS (Razavi, 2006; Emami et al., 2007) as well as BiCMOS (Reynolds et al., 2006). However, none of them achieved a high level of integration like this design where the transmitter and the receiver, the analog/RF circuits, the digital circuits, and the RF passive filters are all included in a single chip.

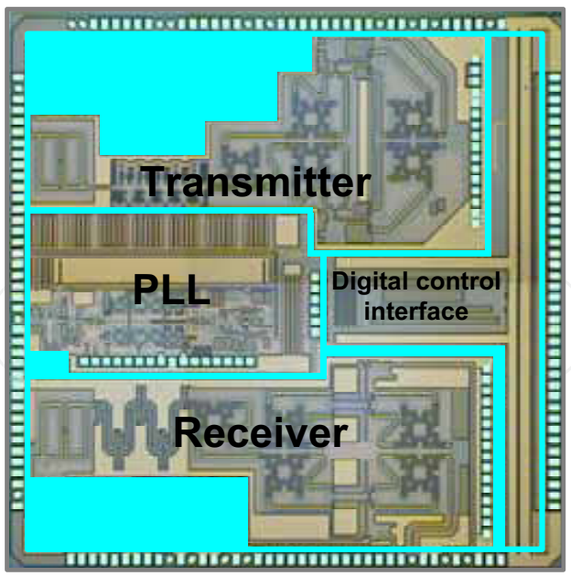
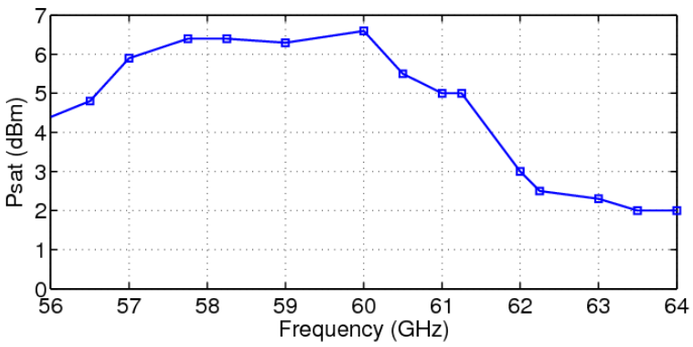


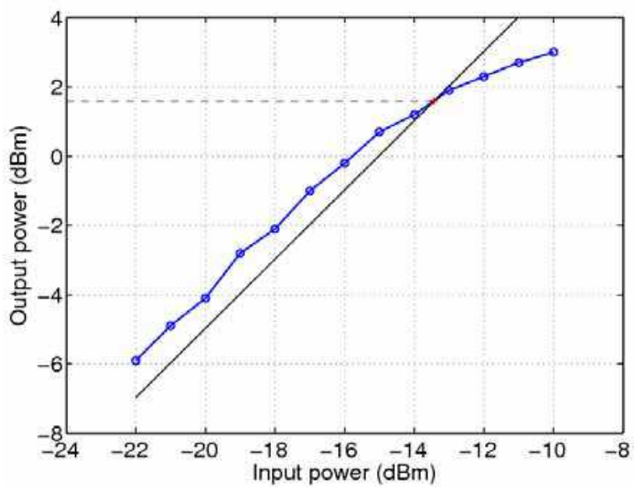
Fig. 24. The 60-GHz single-chip transceiver on 130-nm CMOS technology

The on-chip 60-GHz PLL subsystem was found not function properly even though the functionality and performance of the most challenging circuit, the 60-GHz VCO, had been

verified with measurement results as described in Section 7. An external LO signal was utilized for the purpose of demonstrating the operation of the transmitter and the receiver. The DCI functionality is satisfactory. In all measurement described below, a computer is utilized to control the DCI master. The biasing voltages for the transceiver are set by sending instructions from the computer to the DCI master via an FPGA board.



(a)



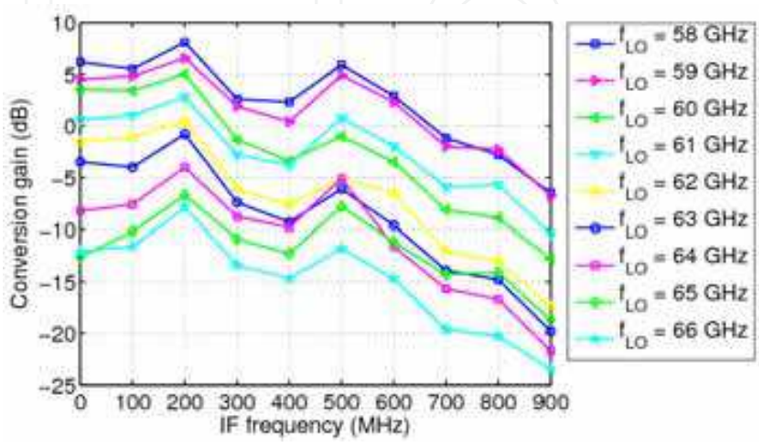
(b)

Fig. 25. Measured output power of the 60-GHz transmitter: (a) saturated output power at different output frequencies, and (b) output power versus input power at 60 GHz

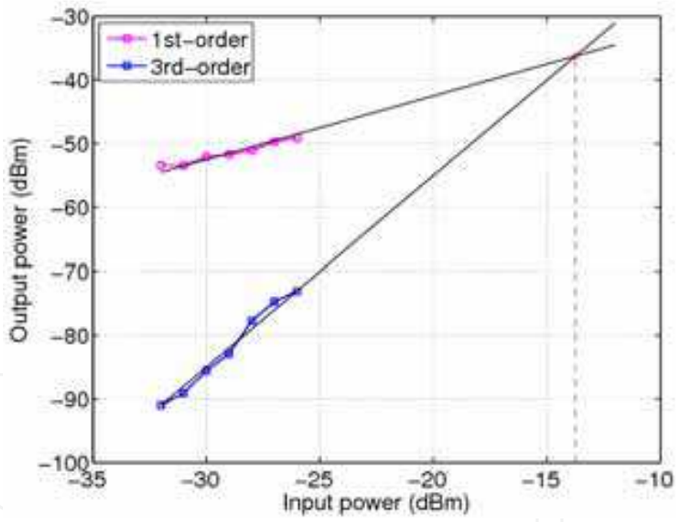
The transmitter consumes a total DC power of 515mW. The transmitting capability of the transmitter is presented in Fig. 25. Fig. 25 (a) shows the saturated output power, P_{sat}, of the transmitter at different frequencies in the 56 to 64GHz band. The output power is at its peak of 6.5dBm for frequencies from 58 to 60GHz. At the high end of the spectrum, the output power is reduced to approximately 2dBm due to the degraded performance of the constituent circuits at high frequency. The output 1-dB compression power was also measured and the collected data is plotted in Fig. 25 (b). At 60 GHz, the output P_{1dB} is 1.6dBm.

The performance of the receiver including its conversion gain and linearity was measured by on-wafer probing. Noise figure measurement was not carried out due to the lack of

appropriate noise sources. The noise figure of the receiver computed from the noise figures and gains of its building blocks is 11.7dB. The receiver consumes a total power of 54mW.
The conversion gain of the receiver is presented in Fig. 26 (a) as functions of the IF frequency. A maximum conversion gain of 8.1 dB is achieved with f_{LO}=58GHz and f_{IF}=200MHz. The conversion gain of the receiver is reduced at high LO frequencies because of the reduced gain of the LNA and the down-conversion mixers at high frequencies.



(a)



(b)

Fig. 26. Measured (a) conversion gain and (b) IIP_3 of the 60-GHz receiver

The linearity of the receiver, quantified by its IIP_3, was estimated from a two-tone test. Two Anritsu MG3690B signal generators were used to generate the two testing tones for the measurement. Due to the lack of another high power 60-GHz signal generator, the LO power was not set up properly for optimum performance of the receiver. Thus the conversion gain of the receiver was reduced substantially in this measurement. It is assumed that the output power of the fundamental tone and the third-order inter-modulation tone were reduced by the same factor so that the IIP_3 computed for the non-optimum operation

conditions closely tracks the IIP_3 of the receiver in its optimum operation conditions. The measured data is plotted in Fig. 26 (b). The IIP_3 of the receiver is approximately -13.74dBm.

10. Conclusion and future work

Recent advances in millimeter-wave electronics have made it possible for a complete wireless transceiver-on-a-chip system to be realized. In order to achieve a low-cost and high-integration solution CMOS is the process of choice. In this chapter we have shown the feasibility of implementing a wireless transceiver on a single chip operating in the millimeter-wave band on CMOS. The 60-GHz CMOS transceiver comprises a transmitter, a receiver, a phase-locked loop, and a digital control interface, and was implemented for the first time on a single silicon die.

The demonstration of the 60-GHz transceiver on a 130-nm CMOS process in this research, even without a working on-chip PLL, has proved the capability of CMOS technology in millimeter-wave circuit domain. However, there is still a large gap, technically and economically, that must be bridged before a truly low-cost, low-power, multi-Gbps CMOS transceiver IC can be achieved. The rest of this section discusses some future work in the process of realization such an IC.

All the circuits in this work was developed on a 130-nm CMOS technology since this was the most advanced CMOS technology characterized up to millimeter-wave frequencies at the time the research started. Owing to the fast scaling speed of CMOS technology, more advanced CMOS processes have been recently put into production by different foundries around the world. Moving the design to a more advanced technology, for example, a 65-nm CMOS technology, promises a better performance of the transceiver.

A directional, steerable phased-array antenna system is an attractive solution to overcome the high path loss at millimeter-wave frequencies and to enable transmission in non-line-of-sight conditions. The configuration of the array, i.e. one or two dimensional array, and the number of the elemental antennae, however, must be carefully determined to achieve the required link budget under certain form factor, cost, and power consumption constraints.

Since the antenna is implemented off-chip, the interface between the antenna and the CMOS transceiver across the chip boundary must be carefully studied. The interconnect between the antenna and the input/output pad on the CMOS chip, whether it is wire-bond or solder bump, must be taken into account during the design of the antenna. Further research must be carried out to understand the characteristic of these interconnects at millimeter-wave frequencies to facilitate the antenna design.

Acknowledgment

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Mobile and Wireless Communications Network Layer and Circuit Level Design

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Mobile and wireless communications applications have a clear impact on improving the humanity wellbeing. From cell phones to wireless internet to home and office devices, most of the applications are converted from wired into wireless communication. Smart and advanced wireless communication environments represent the future technology and evolutionary development step in homes, hospitals, industrial, vehicular and transportation systems. A very appealing research area in these environments has been the wireless ad hoc, sensor and mesh networks. These networks rely on ultra low powered processing nodes that sense surrounding environment temperature, pressure, humidity, motion or chemical hazards, etc. Moreover, the radio frequency (RF) transceiver nodes of such networks require the design of transmitter and receiver equipped with high performance building blocks including antennas, power and low noise amplifiers, mixers and voltage controlled oscillators. Nowadays, the researchers are facing several challenges to design such building blocks while complying with ultra low power consumption, small area and high performance constraints. CMOS technology represents an excellent candidate to facilitate the integration of the whole transceiver on a single chip. However, several challenges have to be tackled while designing and using nanoscale CMOS technologies and require innovative idea from researchers and circuits designers. While major researchers and applications have been focusing on RF wireless communication, optical wireless communication based system has started to draw some attention from researchers for a terrestrial system as well as for aerial and satellite terminals. This renewed interested in optical wireless communications is driven by several advantages such as no licensing requirements policy, no RF radiation hazards, and no need to dig up roads besides its large bandwidth and low power consumption. This second part of the book, Mobile and Wireless Communications: Key Technologies and Future Applications, covers the recent development in ad hoc and sensor networks, the implementation of state of the art of wireless transceivers building blocks and recent development on optical wireless communication systems. We hope that this book will be useful for students, researchers and practitioners in their research studies.

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