Chapter

Application of Random Walk Model for Timing Recovery in Modern Mobile SATCOM Systems

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Abstract

In a modern mobile satellite communication (SATCOM) system, a ground terminal receiver receives a radio frequency signal that is demodulated to generate a baseband digital signal waveform containing a self-clocking bit stream of digital data. The received baseband digital signal waveform is recovered and tracked using a timing recovery loop (TRL). The traditional TRLs use early-and-late gates, digital transition tracking, filter-and-square, and delay-and-multiply functions. In bit timing detection, the bit stream is self-clocking and the timing differential dithers about correct bit timing in the TRLs. For mobile satellite communication environments, the traditional TRLs drop lock when the loop signal-to-noise ratio (SNR) is smaller than a threshold value or the residual Doppler frequency is larger than the operating loop bandwidth. After dropping lock, the traditional TRLs experience long hang up time due to the need to reacquire the timing pulses. Recently, random walk filters (RWF) have been adapted to improve the bit clock locking stability and are applied to recover bit timing information of a digital data stream. This chapter describes random walk model for timing jitter and discusses how RWF solution can address the timing recovery challenges in mobile satellite communication environments.

Keywords: random walk filter (RWF), timing recovery loop (TRL), Mobile communication, bit clock, phase-locked loop (PLL), square-TRL (STRL), 8PSK transmitter/receiver

1. Background and introduction

For mobile environments, current TRLs use traditional TRLs that drop lock at low signal-to-noise ratio (SNR); then, experience long hang up time while reacquiring timing pulses. A potential solution is to introduce RWF into the TRL to reduce drops, and also to shorten reacquisition time. This chapter focuses on random walk model for timing jitter and TRL using RWF [1].

A mobile SATCOM system includes a mobile transmitter, a satellite transponder and a ground terminal receiver as shown in **Figure 1**. The ground terminal receiver receives an RF signal and demodulates the RF signal to generate a baseband (BB)

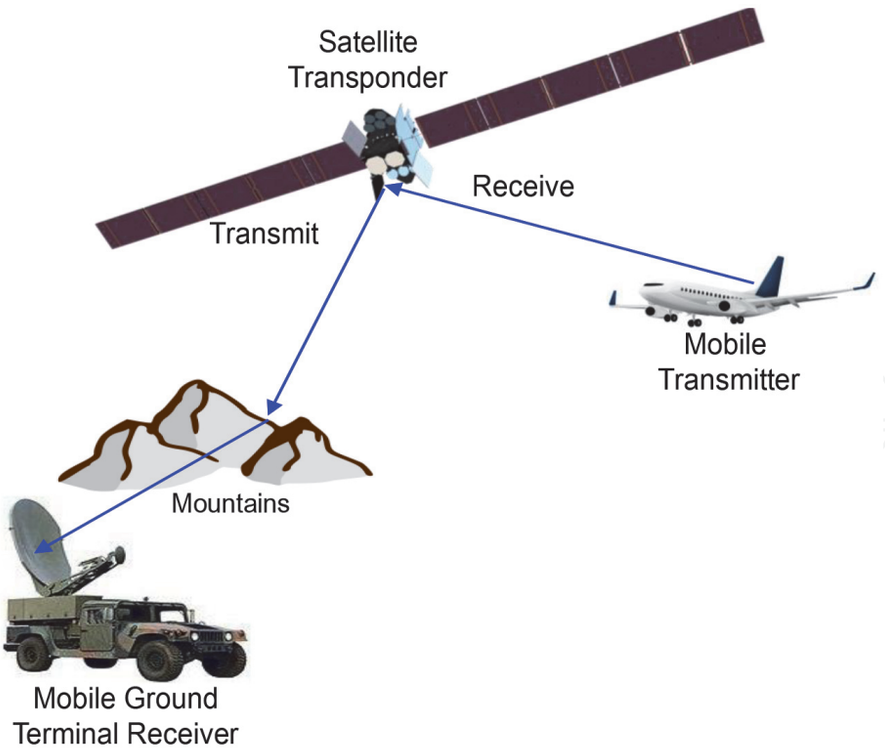

Figure 1.
Mobile satellite communication system.

signal waveform containing a self-clocking binary bit stream of digital data. The generated BB signal waveform is tracked by a TRL. The TRL tracks bit timing of the BB signal waveform and generates timing pulses. The timing pulses are then used in a receiver's data detector for sampling the BB signal waveform at the bit intervals, T_b's, for reconstructing the digital bit stream from the received BB signal waveform. The received BB signal waveform is normally distorted by channel noise causing poorly generated timing pulses and hence poor bit timing recovery leading to poor data bit detection and Bit Error Rate (BER) performance, and hence Symbol Error Rate[1] (SER) degradation. When the TRL loses track, the received binary bit stream is no longer detected. In current communication systems, the received binary bit stream is recovered using traditional TRLs that are subject to bit timing lock drop in the presence of channel noise and fading effects in mobile environment.

The traditional TRLs use Early-and-Late Gates (ELG), Digital Transition Tracking (DTT), Filter-and-Square (FaS), and Delay and-Multiply (DaM) techniques [2–11]. In bit timing detection, the binary bit stream is self-clocking and the timing differential dithers about correct bit timing in the TRLs. For mobile environments (see **Figure 1**), these TRLs drop lock when the timing Loop Signal-to-Noise Ratio (LSNR) is smaller than a threshold value or the residual Doppler frequency is larger than the operating loop bandwidth. After dropping lock, the traditional TRLs experience long hang up time due to the need to reacquire the timing pulses. RWFs have been used for decades in various applications [3–11].

In the past, RWFs have been applied to digital phase synchronization systems. RWFs have been theoretically applied to carrier phase detection where differentials between local references and transmitter carriers results in a phase correction that is unidirectional and constantly circular over 360 degrees [3–6]. Although used for decades, RWFs have not been adapted to improving the bit clock locking stability in

[1] For un-coded Binary Phase Shift Keying (BPSK) the SER is identical to Bit Error Rate (BER).

TRLs. This chapter discusses the RWF based on the Brownian motion process for recovering bit timing information of a binary data stream. The chapter is organized as follow:

- Section 2 presents related works, including PLL modeling using random walk theory[2], Cramér–Rao bound, Square-TRL Using Digital RWF and Advanced TRL Using RWF.

- Section 3 discusses mathematical modeling of timing jitter using random walk process and Cramér–Rao bound for timing jitter.

- Section 4 describes in detail the TRL using RWF, including software implementation and performance of RWF-TRL for 8-PSK communication system.

- Section 5 discusses the results and provides a conclusion of the chapter.

2. Related works

Section 2 describes existing publications related to RWF concept. Section 2.1 presents works related to performance modeling of PLL using random walk theory, Section 2.2 describes the Cramer-Rao Lower Bound that can be used to evaluate the best TRL performance in terms of variance, Section 2.3 discusses the operation and performance of square-TRL using digital RWF and Section 2.4 describes an advanced TRL using RWF approach.

2.1 Performance modeling of PLL using random walk theory

This subsection describes the use of random walk theory on the modeling of all digital PLL, the first-order Bang-Bang PLL and approximation of PLL phase error variance.

2.1.1 The all-digital phase-locked loop

One of the first uses of Random Walk Theory on modeling of phase-locked loop (PLL) was from [4] where the performance of an All-Digital PLL (ADPLL) was analyzed. Here a simple ADPLL for a Non-Return-to-Zero (NRZ) square wave input waveform is shown below in **Figure 2**, with an application to track the sub-carrier frequency for a satellite command system.

In this figure, the square wave signal y(t) is first low pass filtered with a bandwidth of W. The Analog-to-Digital Converter (ADC) will sample at Nyquist rate of 2 W so that there will be $2\ W/f_s$ per period where f_s is the square wave frequency. The phase detector block consists of two elements: (1) the Transition Sampler Selector (TSS) which will output $\pm A$ at each square wave transition, since the sampling error shown as the interval τ seconds can cause the TSS output to be $+A$ or $-A$ depending on where τ is; and (2) an accumulator that will sum m transition samples. Following the Phase Detector, the Sign Detector will be used to add or delete one or more clock pulses, in effect shifting the sampling location of the

[2] The simplest model of Brownian motion is a simple symmetric random walk in one dimension, which is also referred to as random walk (see Section 3).

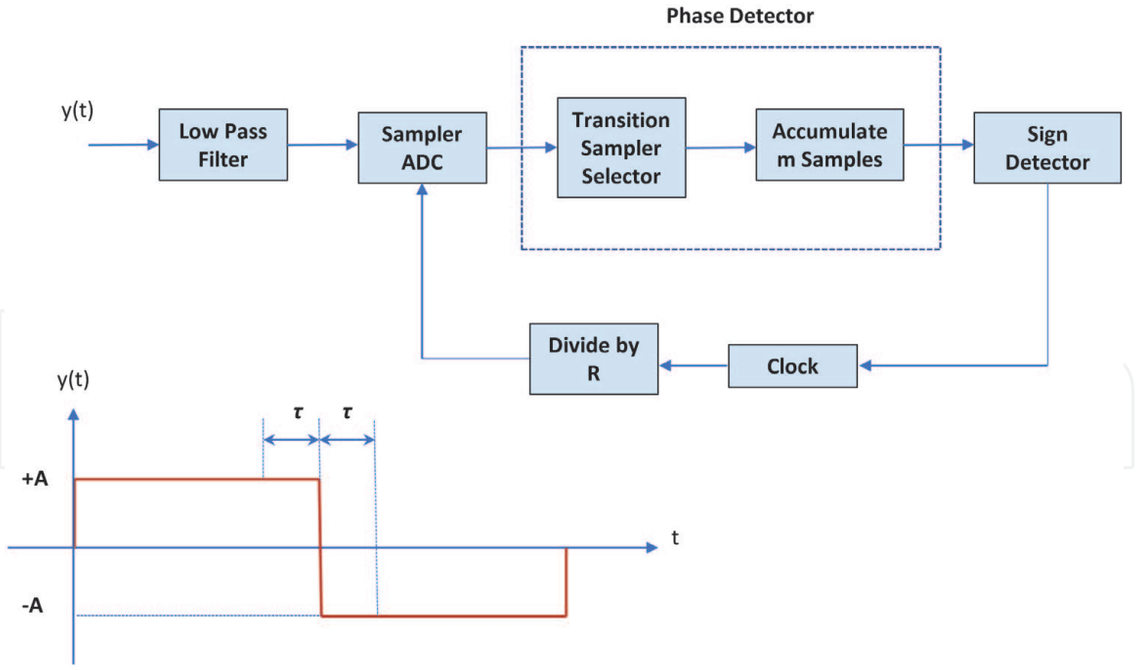

Figure 2.
Block diagram of timing loop update [4].

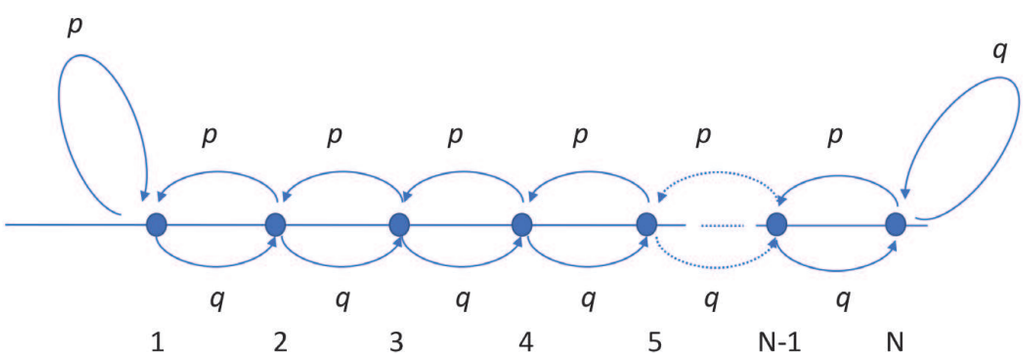

Figure 3.
Reduced state transition diagram showing a random walk [4].

square wave by a multiple of Δ defined as a fraction of the square wave period. The divide-by-R operation will convert the clock rate back to the ADC sample rate ($R = f_c/2$ W) where f_c is the clock frequency.

In the presence of white noise with power density N_0 Watt/Hz, the clock errors normalized to Δ can take on values from $-N, -(N-1), \ldots, -2, -1, 1, 2, \ldots, (N-1), N$ with corresponding transition probabilities. This error model forms a discrete parameter Markov chain with countable number of states, and there are $2N = 1/\Delta$ in one square wave period. The state-transition diagram can be further reduced to N total error states from 2N, by noting that the pairs of states −1 and 1, and −2 and 2, etc., contribute the same squared error. In addition, the transition probabilities are state independent since the square wave amplitude is constant for every state. This independent homogeneous finite aperiodic Markov chain is shown in **Figure 3**.

The above Markov chain is referred to as a "random walk" with the transition probabilities q and p defined in Eq. (1) and (2), respectively, and in terms of signal and noise parameters as shown in Eq. (3):

$$p = erf\left(\rho^{1/2}\right) \tag{1}$$

$$q = 1 - p \tag{2}$$

$$\rho = mA^2/N_0W \tag{3}$$

Where the parameter ρ is the SNR and the erf(.) is defined as in Eq. (4):

$$\mathrm{erf}(x) = \frac{1}{\sqrt{2\pi}}\int_{-\infty}^{x} e^{-t^2/2}dt \tag{4}$$

For this ADPLL, there are three major performance analysis results using the random walk model: the steady-state probabilities, timing error variance, and mean first slip time.

The steady-state probabilities P_k is defined as the probability that the PLL starting in state j is in state k when the number of updates goes to infinity. The expression for P_k is shown in Eq. (5),

$$P_k = \frac{1}{2}\frac{1-q/p}{1-(q/p)^k}\left(\frac{q}{p}\right)^{|k|-1}, k = -N, \ldots, -1, 1, \ldots, N \tag{5}$$

The timing error variance σ_{TE}^2 also has a closed form expression by letting $\alpha = q/p$,

$$\sigma_{TE}^2 = \frac{\Delta^2}{4} + \frac{\Delta^2}{1-\alpha^N}\left\{-N(N+1)\alpha^N + 2\left[\frac{\alpha-(N+1)\alpha^{N+1}}{1-\alpha}\right] + 2\left[\frac{\alpha^2-\alpha^{N+2}}{(1-\alpha)^2}\right]\right\} \tag{6}$$

It is observed from Eq. (6) that as SNR increases, the timing error σ_{TE}^2 converges to $(\Delta/2)^2$ for each value of Δ.

Since it's desirable to keep the timing error small at all times, a useful performance metrics is the Mean First Slip Time (MFST) T^{N+1} which is defined as the expected time for the timing error to exceed some magnitude (usually π or 2π) for the first time when slipping from states ±1 to ± (N + 1). A closed form expression for this metric is shown in Eq. (7) below.

$$T^{N+1} = -\frac{N}{p-q} + \frac{\frac{1}{q}+\frac{1}{p-q}}{\frac{p}{q}-1}\left[\left(\frac{p}{q}\right)^N - 1\right] \tag{7}$$

2.1.2 The first-order bang-bang PLL

The Bang-Bang Phase-Locked Loop (BBPLL) has been widely used for Clock and Data Recovery (CDR) in serial data links and in digital frequency synthesis [5]. A common feature in BBPLL is the Binary Phase Detector (BPD) that quantizes the phase difference between the input data and Voltage-Controlled Oscillator (VCO) clock by generating the early/late phase error information for the Loop Filter (LF). A model for the first-order bang-bang PLL is shown in **Figure 4(a)** where the BPD is represented as a sampler with input as a reference clock and sampled by a VCO. The BBPLL operation in the phase-domain can be summarized by the discrete-time model in **Figure 4(b)**.

In above figures, the behavior of the phase error $\varnothing_n$ can be described by the stochastic difference equation shown in Eq. (8) below:

$$\varnothing_{n+1} = \varnothing_n + \Delta\omega T_0 - K\left(1+\frac{\Delta f}{f_0}\right) sgn\,\varnothing_n + \omega_0\xi_n \tag{8}$$

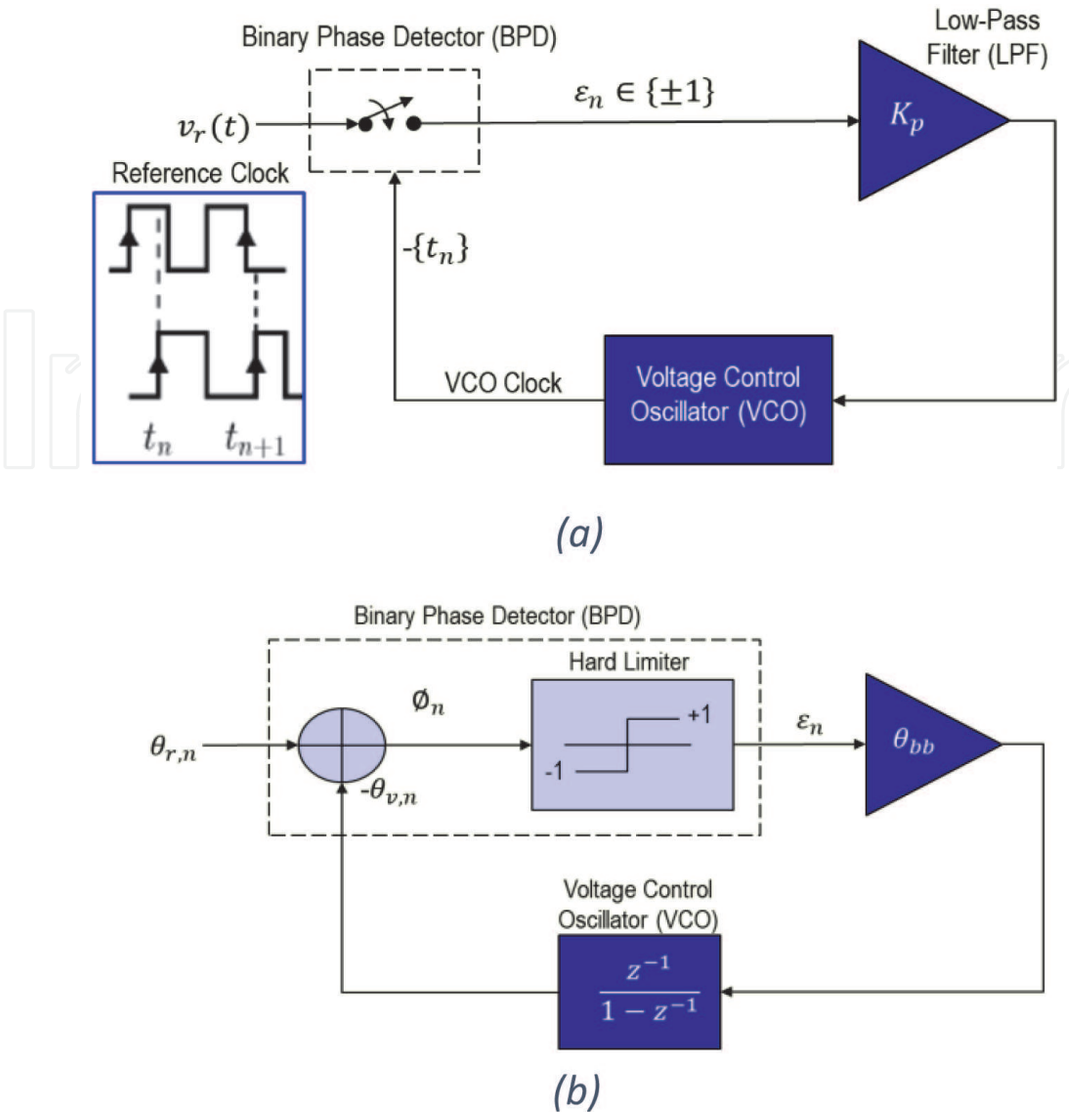

Figure 4.
(a) Model block diagram for the first-order BBPLL [5]. (b) Equivalent phase-domain discrete time model [5].

and corresponding timing jitter is defined as in Eq. (9):

$$\Delta t_{n+1} = \begin{cases} \Delta t_n + \Delta T - K + \xi_n, \Delta t_n \geq 0 \\ \Delta t_n + \Delta T + K + \xi_n, \Delta t_n \leq 0 \end{cases} \quad (9)$$

where$\Delta T = \Delta f / f_0^2$ is the period deviation due to frequency offset[3], K is the bang-bang phase step, and ξ_n is a sequence of zero-mean independent and identically distributed (i.i.d.) random variables (RVs). This follows a random walk (RW) model starting at some origin (n = 0) with ξ_n being the step RV with a distribution F. This RW model is sign dependent since the next step depends on the sign of the current state, thus called Sign-Dependent Random Walk (SDRW) model. Furthermore, if we assume that $\mu_+ = \Delta T - K$ and $\mu_- = \Delta T + K$ are Gaussian RVs with variance $\sigma^2_{+/-} = \sigma^2$ then the timing jitter process can be viewed as Sign-Dependent Gaussian Random walk (SDGRW).

PLL design questions are often centered around how much jitter is transferred from the reference clock, how much jitter is generated by the loop itself, and what is the minimum Root Mean Square (RMS) timing jitter. The first two can be answered

[3] The notation ΔT for frequency offset is not conventionally consistent but preserved from [5].

by examining the static timing offset error derived in [5]. A static timing offset is a significant problem in a BBPLL-based CDR circuit because it results in the incoming data no longer sampled at the center of the data eye, thus increasing the bit error rate. A closed form expression for static timing offset error is shown in Eq. (10) below.

$$\Delta t_{stat} = \Delta T + \sigma G_1\left(\frac{K-\Delta T}{\sigma}\right) + \sigma G_1\left(\frac{K+\Delta T}{\sigma}\right) \tag{10}$$

Where

$$G_k(x) = \sum_{n=1}^{\infty} g_k(n,x) \tag{11}$$

and

$$g_1(n,x) = \frac{1}{\sqrt{2\pi n}} e^{-nx^2/2} - \frac{1}{2}x \cdot erfc\left(\sqrt{\frac{n}{2}}x\right) \tag{12}$$

As shown in Eq. (10), the behavior of the static timing offset error vs. frequency offset ΔT at K = 1 can be determined by setting $\Delta T>0$ and letting σ to be larger than 1, the combined effect of frequency offset and clock jitter causes the static timing offset to increase from its jitter-free level. But by setting $\Delta T>0$ and letting σ be much less than 1, the static timing offset does not notably increase for a small enough σ, even with a moderate frequency offset.

The above third question can be answered by examining the variance of timing jitter error derived in [5]. A closed form expression for timing jitter error variance is shown in Eq. (13):

$$\sigma_{\Delta t}^2 = \frac{K^2}{3} + \sigma^2 + \sigma^2 G_2\left(\frac{K-\Delta T}{\sigma}\right) + \sigma^2 G_2\left(\frac{K+\Delta T}{\sigma}\right) \tag{13}$$

where

$$G_2(n,x) = \frac{1}{2}\left(nx^2+1\right) erfc\left(\sqrt{\frac{n}{2}}x\right) - \sqrt{\frac{n}{2\pi}} x e^{-nx^2/2} \tag{14}$$

The plot of the timing jitter error standard deviation $\sigma_{\Delta t}$ for various values of timing jitter noise σ and frequency offsets ΔT can be generated using Eq. (13) as shown in **Figure 5**. For small jitter noise, the hunting jitter dominates so RMS timing jitter error is approximately constant and approaching an asymptote. Increasing jitter noise causes RMS timing jitter error to rise because the effect of the Gaussian clock jitter and the resulting overload jitter becomes gradually apparent. For large jitter noise, overload jitter dominates, and shows a linear increase on the logarithmic scale.

Finally, an important parameter is the optimal bang-bang phase step K to achieve a minimum timing jitter variance. The expression for the optimum phase step is:

$$K_{opt}^2 = \Delta T^2 + \left(2\sigma^4 \lambda \Delta T^2\right)^{1/3} + \left(\sigma^8 / \left(24\lambda \Delta T^2\right)\right)^{1/3} \tag{15}$$

where $\lambda = 1 + \sqrt{1 - \sigma^4\left(72\Delta T^4\right)}$. The trade-off curves can be generated by substituting Eq. (15) into Eq. (13), and they can be used to optimize a BBPLL design.

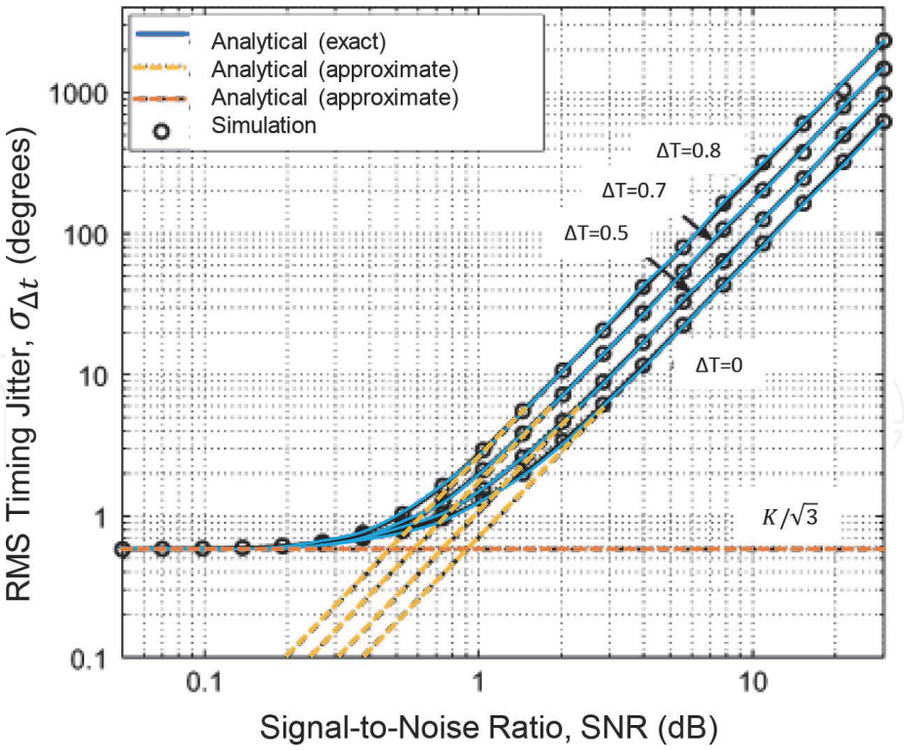

Figure 5.
RMS timing jitter error vs. SNR [5].

2.1.3 Approximation of PLL phase-error variance

Approximations for the expression of phase error variance due to nonwhite frequency noise with finite loop propagation delay have been created by Norimatsu and Ishida [7]. The PLL phase error σ^2_{total} is expressed as a summation of the phase error variance due to phase noise, σ^2_{PN}, and the phase error variance due to shot noise σ^2_{SN} given by [7]:

$$\sigma^2_{total} = \sigma^2_{PN} + \sigma^2_{SN} \tag{16}$$

$$\sigma^2_{total} = \int_{-\infty}^{\infty} S_{PN}(f)|1 - H(f)|^2 df + \frac{e}{M\,R\,k_s P_s}\int_{-\infty}^{\infty} |H(f)|^2 df \tag{17}$$

Where S_{PN} is the double-sided power spectral density (PSD) of the phase noise, H(f) is the closed loop transfer function of the PLL, e [A sec] is the electron charge, P_s [W] is the received optical power, R [A/W] is the photon detector responsivity, M is 4 for BPSK homodyne detection and 2 for other schemes and k_s is the optical power splitting ratio to the quadrature-arm.

2.2 Cramér–Rao bound (CRB)

In information theory and statistical analysis, the Cramer-Rao Lower Bound (CRLB) is often used to evaluate the best performance in terms of variance of any unbiased parameter estimator, whether the parameter to be estimated is random or deterministic but unknown. An unbiased estimator that achieves this lower bound is said to be statistically efficient, achieves the lowest possible mean squared error among all unbiased methods and is therefore called the minimum variance unbiased estimator (MVUE). However, there is no guarantee that an estimator exists that will achieve the CRLB. This may occur if an estimator exists, but its variance is strictly greater than the CRLB.

Given that $\hat{\boldsymbol{\theta}}(\boldsymbol{r})$ is the multiple-parameter estimator of $\boldsymbol{\theta} = [\boldsymbol{\theta_0}, \boldsymbol{\theta_1}, \ldots, \boldsymbol{\theta_{M-1}}]^T$ based on the observation data vector $\boldsymbol{r} = [\boldsymbol{r_0}, \boldsymbol{r_1}, \ldots, \boldsymbol{r_{N-1}}]^T$, the CRLB for this problem is given by Eq. (18):

$$\boldsymbol{CRLB} = \boldsymbol{E_{r,\theta}}\left[\left(\hat{\boldsymbol{\theta}}(\boldsymbol{r}) - \boldsymbol{\theta}\right)\left(\hat{\boldsymbol{\theta}}(\boldsymbol{r}) - \boldsymbol{\theta}\right)^T\right] \geq \boldsymbol{J_T^{-1}} \tag{18}$$

Where $\boldsymbol{J_T^{-1}}$ is the "total" Fisher Information Matrix (FIM), defined by:

$$\boldsymbol{J_T} = \boldsymbol{E_{r,\theta}}\left\{\left[\frac{\partial}{\partial \boldsymbol{\theta}} \boldsymbol{ln}\, \boldsymbol{f}(\boldsymbol{r}, \boldsymbol{\theta})\right]\left[\frac{\partial}{\partial \boldsymbol{\theta}} \boldsymbol{ln}\, \boldsymbol{f}(\boldsymbol{r}, \boldsymbol{\theta})\right]^T\right\} \tag{19}$$

Where $\boldsymbol{f}(\boldsymbol{r}, \boldsymbol{\theta})$ is the joint probability density function (pdf) of $\boldsymbol{r}$ **and** $\boldsymbol{\theta}$. The estimation error variance of each estimate of $\boldsymbol{\theta_i}$ can be taken from the diagonal term of the $\boldsymbol{J_T^{-1}}$ matrix. Since $\boldsymbol{f}(\boldsymbol{r}, \boldsymbol{\theta}) = \boldsymbol{f_{r|\theta}}(\boldsymbol{r}|\boldsymbol{\theta})\boldsymbol{f_\theta}(\boldsymbol{\theta})$ where $\boldsymbol{f_{r|\theta}}(\boldsymbol{r}|\boldsymbol{\theta})$ is the conditional pdf of $\boldsymbol{r}$ given $\boldsymbol{\theta}$, and $\boldsymbol{f_\theta}(\boldsymbol{\theta})$ is the a-priori pdf of $\boldsymbol{\theta}$. So the total FIM can be separated into two distinct parts representing deterministic and random parts for each type of estimator is shown in Eq. (20):

$$\boldsymbol{J_T} = \boldsymbol{E_\theta}[\boldsymbol{J_\theta}] + \boldsymbol{J_{ap}} \tag{20}$$

Where the deterministic FIM part is:

$$\boldsymbol{J_\theta} = \boldsymbol{E_\theta}\left\{\left[\frac{\partial}{\partial \boldsymbol{\theta}} \boldsymbol{ln}\, \boldsymbol{f_{r|\theta}}(\boldsymbol{r}|\boldsymbol{\theta})\right]\left[\frac{\partial}{\partial \boldsymbol{\theta}} \boldsymbol{ln}\, \boldsymbol{f_{r|\theta}}(\boldsymbol{r}|\boldsymbol{\theta})\right]^T\right\} \tag{21}$$

and the a-priori FIM for the random parameter estimator is:

$$\boldsymbol{J_{ap}} = \boldsymbol{E_\theta}\left\{\left[\frac{\partial}{\partial \boldsymbol{\theta}} \boldsymbol{ln}\, \boldsymbol{f_\theta}(\boldsymbol{\theta})\right]\left[\frac{\partial}{\partial \boldsymbol{\theta}} \boldsymbol{ln}\, \boldsymbol{f_\theta}(\boldsymbol{\theta})\right]^T\right\} \tag{22}$$

For each problem, the appropriate FIM will need to be calculated accordingly. The inversion of the composite FIM will result in the CRLB.

2.3 Square-TRL using digital RWF

Digital filter with Square-TRL (DF-STRL) has been proposed and discussed in [6]. Due to its simplicity and hang-up-free filtering features, DF-STRL has been used by satellite ground terminals for Pulse Amplitude Modulation (PAM), Quadrature Amplitude Modulation (QAM) and Phase Shift-Keying (PSK) waveforms operating at high data rates. A typical DF-STRL architecture is shown in **Figure 6**, where the integer N is selected to be 4.

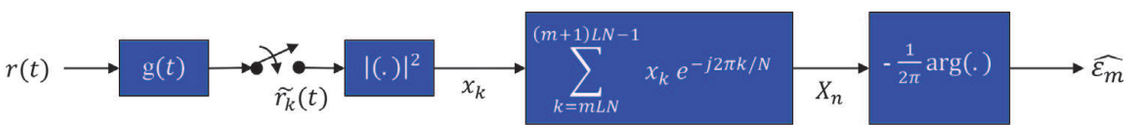

Figure 6.
Digital filter and square-TRL (DF-STRL) [6].

If one assumes that the mean of the timing estimate $\hat{\varepsilon_m}$ is zero, the timing jitter (or timing variance of the timing estimate), σ_τ^2, is defined as:

$$\sigma_\tau^2 = E\left\{(\hat{\varepsilon_m})^2\right\} = \frac{1}{(2\pi)^2} E\left\{(\arg(X_n))^2\right\} = \frac{1}{(2\pi)^2} E\left\{\left(\frac{\mathrm{Im}(X_n)}{\mathrm{Re}\,(X_n)}\right)^2\right\} \tag{23}$$

Reference 6 shows that the timing jitter, σ_τ^2, for DF-STRL consists of three components, namely

- Timing jitter generated by (Signal x Signal)–This term is referred to as self-noise term: σ_{SxS}^2
- Timing jitter generated by (Signal x Noise)–This term is referred to as Squaring Loss (SL) term: σ_{SxN}^2
- Timing jitter generated by (Noise x Noise): σ_{NxN}^2

Mathematically, the timing jitter, σ_τ^2, for DF-STRL can be expressed as:

$$\sigma_\tau^2 = \sigma_{SxS}^2 + \sigma_{NxN}^2 + \sigma_{SxN}^2 \tag{24}$$

Analysis shown in [6] showed that the timing estimate $\hat{\varepsilon_m}$ is un-biased, which means that the average $\hat{\varepsilon_m}$ coincides with ε_m. The estimation accuracy depends on several loop parameters, including Symbol SNR, observation interval L_0 and the pulse shaping filter g(t). The timing jitter in Eq. (24) can be put in the form ([11], Section 7.6.2):

$$\sigma_\tau^2 = \frac{T}{L_0}\left[K_{SxS} + K_{SxN}\left(\frac{E_S}{N_0}\right)^{-1} + K_{NxN}\left(\frac{E_S}{N_0}\right)^{-2}\right] \tag{25}$$

where T is the symbol duration, $\frac{E_S}{N_0}$ is the symbol SNR, and K_{SxS}, K_{SxN} and K_{NxN} are the coefficients depending on the symbol alphabet and the pulse shaping filter g(t). The pulse shaping filter g(t) is usually Root-Raised-Cosine filter with roll-off α.

2.4 Advanced TRL using RWF

Recently, a small team of Aerospace engineers developed an innovative approach to recover the timing information from a received binary data stream [1]. The proposed approach uses:

- A "RWF counter" for counting early, nominal and late arrivals of data transition pulses of an input binary data stream
- The output of the RWF provides magnitude counts that are compared to a Threshold Value (TV) that when exceeded by the magnitude counts results in a delay adjustment of the generated Adjusted Timing Pulses (ATPs)
- The ATPs are eventually catching up with the actual timing clocks
- When ATPs caught up, no delay adjustment will be made allowing ATPs to synchronize with the actual bit timing for maintaining bit timing lock

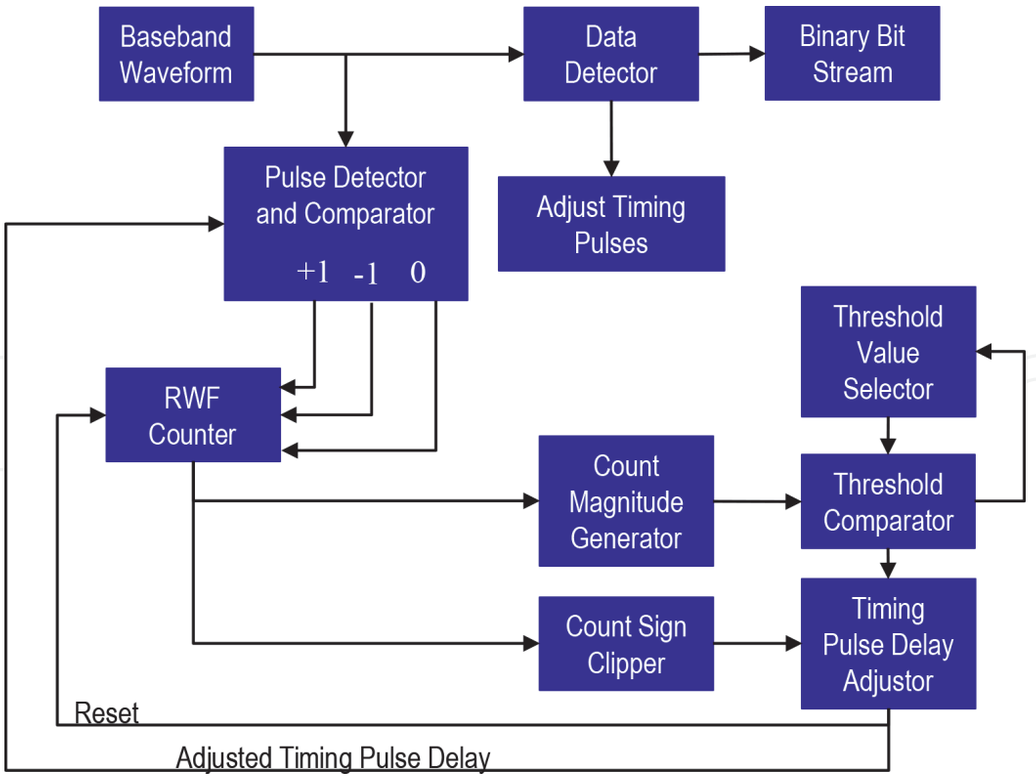

Figure 7.
RWF TRL [1].

- The ATPs are used by a data detector for reliable data detection and reconstruction of the binary bit stream.

With the proposed RWF approach, the threshold value "TV" can be adaptively adjusted for reducing drop lock rates in the presence of changing channel environments. **Figure 7** illustrates the proposed RWF approach for timing recovery. Section 4 discusses in depth the proposed RWF implementation approach and presents simulation results for 8PSK Modulator-Demodulator (MODEM).

3. Mathematical modeling of timing jitter using random walk process

The Wiener process was introduced as a mathematical model of Brownian motion describing a random, but continuous motion of a particle, subjected to the influence of a large number of chaotically moving molecules of the liquid. The simplest model of Brownian motion is a simple symmetric random walk in one dimension (aka random walk) [12]. It also has been shown that Brownian motion with zero drift is the limiting case of random walk [13]. This section describes the mathematical random time walk model for charactering the timing jitter in an Additive White Gaussian Noisy channel and the corresponding Cramér–Rao bound for timing jitter.

3.1 Mathematical modeling of random time walk

References [3, 5] discuss a Random Time Walk (RTW) model, which can be captured in the following **Figure 8**. The RTW model includes a binary data stream $\{a_k\}$ that is independent identically distributed data symbols (−1 or 1), a timing

Figure 8.
Random time walk model [3].

offsets τ timing, a channel impulse response h(t), an Additive Gaussian White Noise (AWGN) source and channel output y(t).

The RTW model used for the modeling of timing jitter and performance analysis shown in **Figure 8** [3], can be expressed mathematically as:

$$\boldsymbol{y(t)} = \sum_{\boldsymbol{l=0}}^{\boldsymbol{N-1}} \boldsymbol{a_l h(t - lT - \tau_l)} + \boldsymbol{n(t)} \tag{26}$$

where T is the bit period, $\boldsymbol{a_l \epsilon \{\pm 1\}}$ are the N i.i.d. and equally likely data symbols, $\boldsymbol{h(t)}$ is the channel impulse response, $\boldsymbol{n(t)}$ is additive white Gaussian noise, and $\boldsymbol{\tau_l}$ is the random timing offset for the l-th symbol. This timing offset model can also be expressed as:

$$\boldsymbol{\tau_{k+1}} = \boldsymbol{\tau_0} + \boldsymbol{(k+1)\Delta T} + \sum_{\boldsymbol{l=0}}^{\boldsymbol{k}} \boldsymbol{w_l} \tag{27}$$

where $\boldsymbol{\tau_0}$ is the initial timing offset and zero-mean Gaussian random variable with variance $\boldsymbol{\sigma^2_{\tau_0}}$, $\boldsymbol{\Delta T}$ is the frequency offset parameter zero-mean Gaussian random variable with variance $\boldsymbol{\sigma^2_{\Delta T}}$, $\{\boldsymbol{w_l}\}$ characterizes a random walk and are i.i.d. zero-mean Gaussian random variables of variance $\boldsymbol{\sigma^2_w}$ which determines the severity of the random walk.

3.2 Cramér–Rao bound (CRB) for timing jitter

The RTW model described in Section 3.1 will be used for the CRLB derivation. To eliminate out-of-band noise at the receiver, the received waveform $y(t)$ is filtered by a front-end filter with impulse response $f(t)$ to get the waveform $r(t)$, which will be sampled at instant kT to get baud-rate sample $\{r_k\}$ given by:

$$r_k = \sum_{l=0}^{N-1} a_l h_1(kT - lT - \tau_l) + n_k = x_k + n_k \tag{28}$$

Where $h_1(t) = h(t) * f(t)$, $x = [x_0, x_1, \ldots, x_{N-1}]^T$ is the vector of signal component of r_k, and n_k are zero-mean i.i.d. normal random variables with variance σ^2. In this timing jitter models, the random parameters to be estimated are $a = [a_0, a_1, \ldots, a_{N-1}]^T$ is the vector of transmitted symbols, and $\tau = [\tau_0, \tau_1, \ldots, \tau_{N-1}]^T$ is the vector of timing offsets.

For the CRLB computation, the parameter vector $\theta = \left[\tau^T \, a^T\right]^T$ and $\hat{\theta} = \left[\hat{\tau}^T \hat{a}^T\right]^T$. From Section 2.2,

$$J_T = \begin{bmatrix} J_T^{\tau} & 0 \\ 0 & J_T^{a} \end{bmatrix} \tag{29}$$

represent the total FIM so that the joint estimation is decoupled, and to get the CRLB on timing estimation it is sufficient to evaluate and invert J_T^{τ} which is given by

$$J_T^{\tau} = \frac{1}{\sigma_w^2}\begin{bmatrix} \beta_2 & -1 & 0 & \dots & 0 \\ -1 & \lambda & -1 & \ddots & \vdots \\ 0 & \ddots & \ddots & \ddots & 0 \\ \ddots & \ddots & -1 & \lambda & -1 \\ 0 & \ddots & 0 & -1 & \lambda - 1 \end{bmatrix} \tag{30}$$

Where $\lambda = 2 + C\frac{\sigma_w^2}{\sigma^2 T}$, $\beta_2 = \beta_1 + C\frac{\sigma_w^2}{\sigma^2 T}$, and $\beta_1 = \left(\frac{N^2-N-1}{N^2} + \frac{\sigma_w^2}{\sigma_{\tau_0}^2} + \frac{\sigma_w^2}{N^2\sigma_{\Delta T}^2}\right)$, and $C = \left(\frac{2\pi^2}{3} - 1\right)$. The a-priori information parameters $\sigma_{\tau_0}^2$ and $\sigma_{\Delta T}^2$ represent the uncertainty of the initial timing offset and frequency offset, being zero would mean perfect knowledge of these two quantities which is not practical, and the estimation problem is simply that of estimating a random walk. Inverting (30) to get the CRLB for each τ_i leads to

$$\frac{E\left[\left(\hat{\tau}_i(r) - \tau_i\right)^2\right]}{T^2} \geq h \cdot f(i) \tag{31}$$

where

$$h = \frac{\sigma_{\varepsilon}^2}{T^2}\frac{\eta}{\eta^2 - 1} \tag{32}$$

is the stead state value of the CRLB,

$$f(i) = \tanh\left(\left(N + \frac{1}{2}\right)\ln\eta\right)\left[1 - \frac{\sinh\left(\left(N - 2i - \frac{3}{2}\right)\ln\eta\right)}{\sinh\left(\left(N + \frac{1}{2}\right)\ln\eta\right)}\right] \tag{33}$$

and $\boldsymbol{\eta} = \frac{\lambda + \sqrt{\lambda^2 - 4}}{2}$.

The CRLB derived applies to timing recovery systems in general. In practice, timing recovery systems usually involve phase locked loops. A traditional PLL is typically used for timing recovery, and the receiver employs a timing-error detector (TED) to arrive at timing-error estimates. For simplicity, a first-order PLL is employed which updates its estimate according to

$$\hat{\tau}_{k+1} = \hat{\tau}_k + \alpha\hat{\epsilon}_k \tag{34}$$

where α is the PLL gain, and $\hat{\epsilon}_k$ is the detector estimate of the estimation error. Instead of feeding the TED decisions about the received symbols, if we allow it to have access to the actual transmitted symbols, then we have a trained PLL. The performance of trained PLL gives a heuristic lower bound for the performance of receiver structures that use the PLL for timing recovery.

In **Figure 9**, the steady state CRB and the performance of the trained PLL are plotted for the following system parameters: $\frac{\sigma_{\varepsilon}}{T} = 0.5\%$, block length N = 500, and the PLL performance being averaged over 1000 trials [8]. As seen in the figure, the performance of the PLL is a strong function of the gain parameter α, and therefore it has to be optimized for each SNR. The PLL error variance is plotted for various

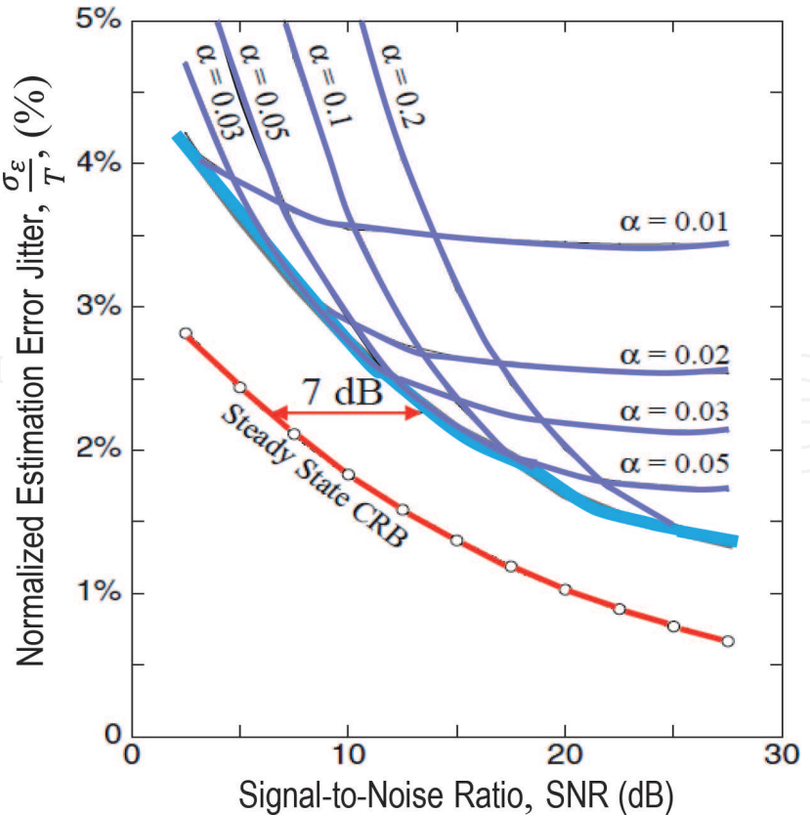

Figure 9.
Trained PLL and the CRLB [8].

values of α. Taking the minimum of the error variance over all α gives us the best performance we can expect using the trained PLL. We see that the trained PLL is about 7 dB away from the CRB. This gap of 7 dB has to be put in perspective by the fact that the CRB is not attainable in this case. For the CRB to be attainable, the a-posteriori density $f_{r|\theta}(r|\theta)$ needs to be Gaussian, which is not the case here.

4. Timing recovery using RWF

The most commonly used TRLs in existing wireless and satellite communications systems are DF-STRL, Early-and-Late Gate, Digital Transition Tracking, and Delay-and-Multiply TRLs [6, 9–11]. For mobile environments, these TRLs drop lock when the loop signal-to-noise ratio (SNR) is smaller than the threshold value SNR or the residual Doppler frequency is larger than the operating loop bandwidth. When "dropped lock", these timing loops experience a long "hang-up" time due to reacquisition and locking behavior of the timing clock. As discussed in Section 2.3 on the related works for DF-STRL, a form of digital RWF was proposed for use with square TRL. This DF-STRL suffers squaring loss caused by squaring mechanism used by the loop. This section explores the advanced TRL using RWF.

4.1 RWF concept for timing recovery

The RWF-TRL concept derived from the following principles:

- Principle 1: Input binary signal waveform is compared in time with locally generated and suitably delayed timing pulses to produce lead/lag signals to increment/decrement a timing counter.

- Principles 2: When timing counter output exceeds a positive or negative threshold, the delay for timing pulses is adjusted accordingly.

- Principle 3: Without timing errors, an appropriately selected threshold value allows the lead and lag signals to cancel out in time, thus retaining the correct timing pulses.

The block diagram, shown in **Figure 10**, describes the above principles pictorially. The received binary data is a square wave with amplitude varying between +1 and −1 with time duration T in second, which is inversely proportional to the communication data bit rate R in bit per second.

4.2 Software implementation of RWF TRL

The major Software Blocks (SWB) required for implementing the above three principles are:

- SWB 1: Pulse detection and comparison block converts input baseband digital signal waveform to data transition pulses and compares them to timing pulses to generate lead/lag signals.

- SWB 2: RWF counter block generates a running count that is incremented/decremented by the lead/lag signals.

- SWB 3: Threshold comparison block generates exceedance signal when magnitude of running count is greater than a selected threshold.

- SWB 4: Timing pulse delay adjustment block uses sign of running count to adjust timing pulses when triggered by exceedance signal.

Figure 11 presents a software architecture for implementation of the three principles described in Section 4.1. The threshold value is derived based on a threshold selection process that depends on the channel environment. Either a training sequence or a priori knowledge of the channel propagation conditions may

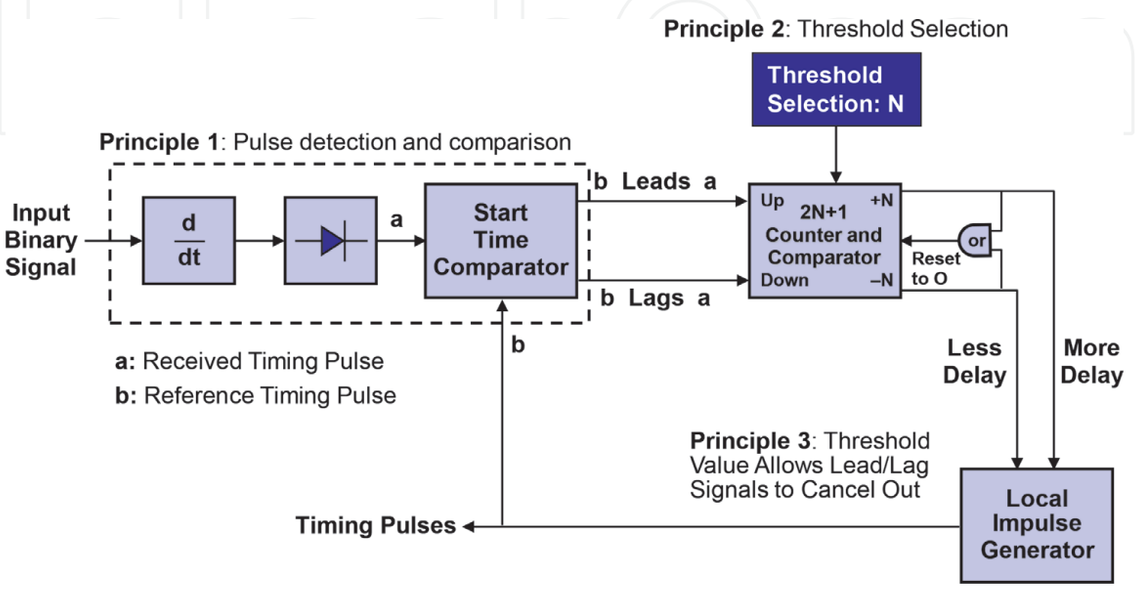

Figure 10.
RWF concept for timing recovery.

be needed to set the threshold. Alternatively, an algorithm can be provided to adaptively select a threshold value to compensate for channel impairments.

Figure 12 describes the "Pulse Detection and Comparison Block", or SWB 1. This SWB1 consists of the following functions:

- Converts input baseband digital signal waveform to data transition pulses delayed by half of the search window size, W.
- Generates timing pulses that are delayed by the adjusted timing pulse delay that is input to the block.
- Counts number of data transition pulses that are within W from each successive timing pulse and keep track of the delay of the first data transition pulse.
- Calculates lead/lag time of the first data transition pulse as the delay time minus half of the search window size, and lead/lag signal as the sign of the lead/lag time.
- Outputs a non-zero lead/lag signal if there is one, and only one, data transition pulse within the search window, thus eliminating much of the noise-caused ambiguity.

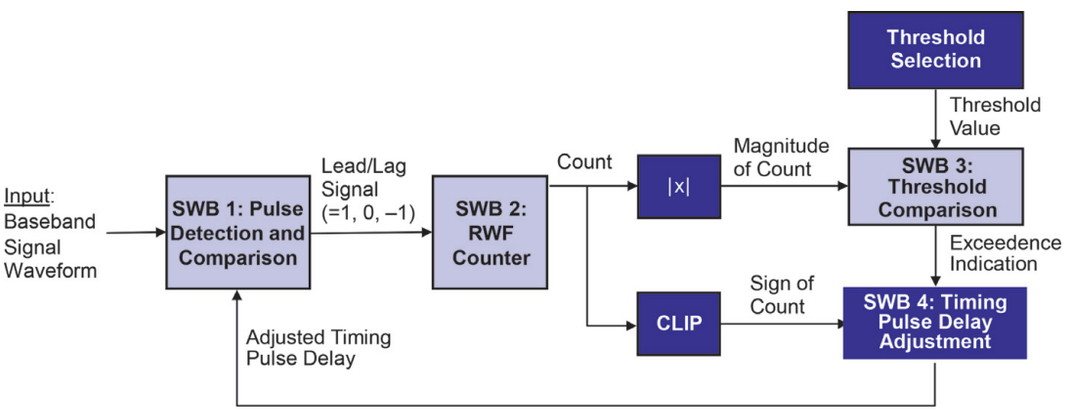

Figure 11.
Software architecture of advanced TRL using RWF.

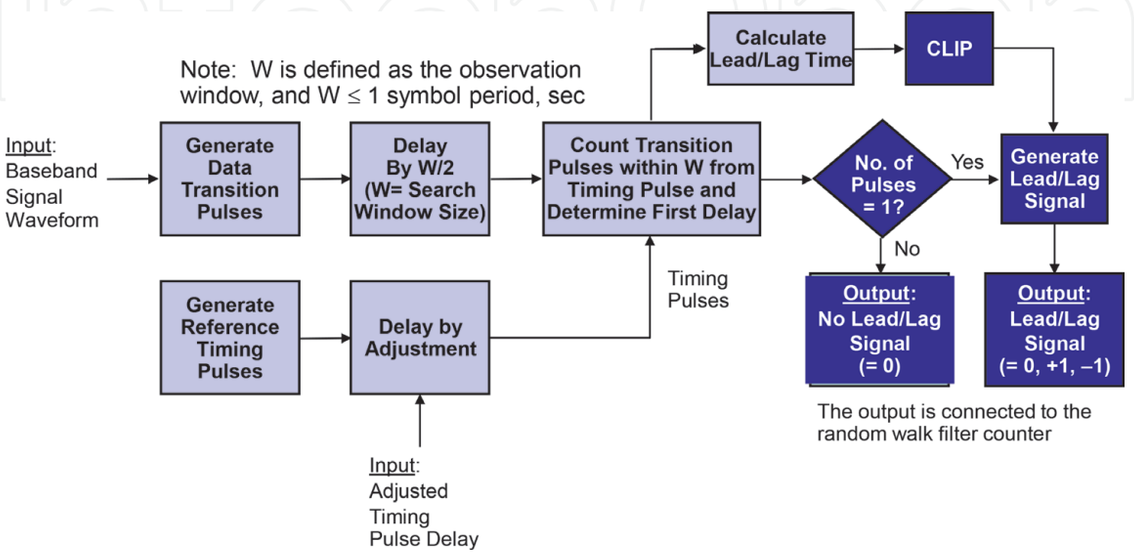

Figure 12.
SWB 1 implementation of pulse detection and comparison.

4.3 Performance of RWF TRL

Signal Processing Work (SPW) implementation of the proposed RWF TRL for 8-PSK modem is described in **Figure 13**. The proposed implementation includes the following blocks:

- 8PSK transmitter block generates signals modulated by sine and cosine waveforms.
- AWGN generator block adds Gaussian random noise to the 8PSK signals.
- Demodulator with ideal phase tracking converts the 8PSK signals to baseband.
- Combination of low pass filter (LPF) and hard-limiter generates a binary data stream from the 8PSK signals.
- RWF TRL block generates clock signals (timing pulses).
- Sum dump and hold block uses the clock signals to integrate the baseband 8PSK signals.
- 8PSK detector puts the integrated signals through 8PSK slicer to reconstruct the data stream.
- SER estimator compares the original data stream with the reconstructed data stream to detect symbol errors.

SPW-simulated SER curve with imperfect timing recovery is shown in **Figure 14**. This SER curve was obtained under the following operational conditions, which is not optimized in terms of search window and threshold value used by the counter:

- Back-to-back Modem with no transponder or amplifier in between, i.e., no Amplitude Modulation-to-Amplitude Modulation (AM-AM) and Amplitude Modulation-to-Phase Modulation (AM-PM) distortions.
- Carrier frequency: 5000 Hz

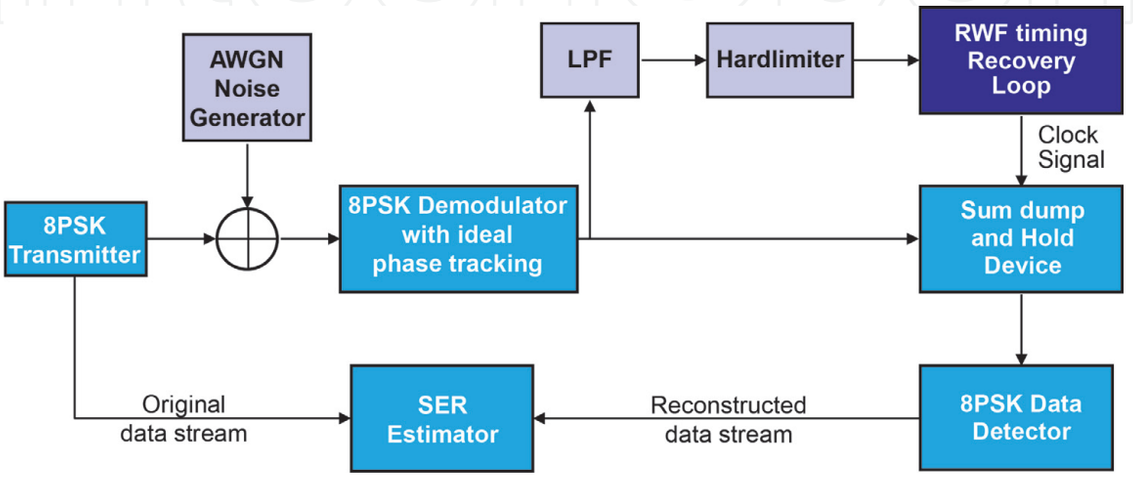

Figure 13.
Simulation set-up for 8PSK modem with RWF-TRL.

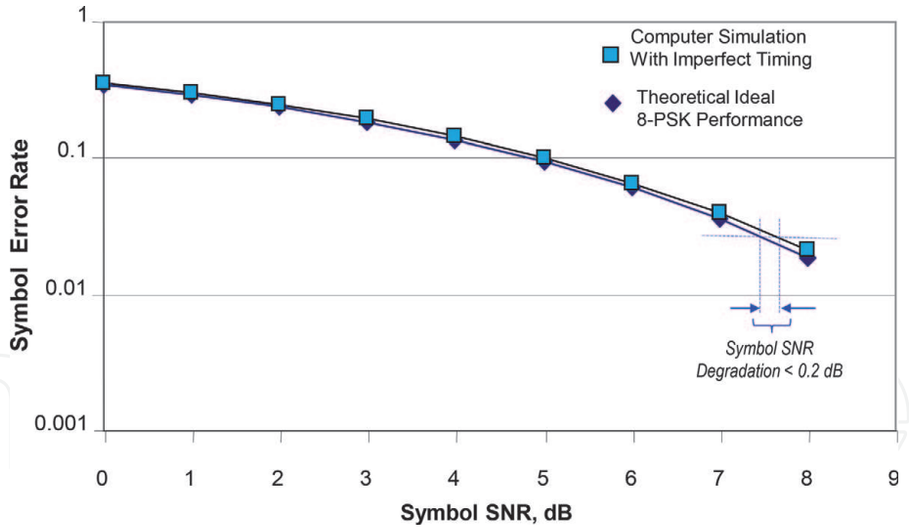

Figure 14.
8-PSK symbol error rate simulation with RWF TRL.

- Symbol rate: 1000 sps
- Number of samples per symbol: 50
- Search window size: 10 samples
- Threshold for counter: 10 counts

For symbol SNR greater than 2 dB, the theoretical SER for 8PSK can be accurately estimated from the following Eq. [9–10]:

$$SER \approx 2Q\left\{\sqrt{2.\gamma_s}\, sin\left(\frac{\pi}{8}\right)\right\} \tag{35}$$

where is γ_s the symbol SNR and $Q(x)$ is the Q-function given by:

$$\mathrm{Q}(x) = \frac{1}{\sqrt{2\pi}}\int_x^{\infty} e^{\left(-t^2/2\right)} dt = 1 - \mathrm{erf}(x) \tag{36}$$

As shown in **Figure 14**, the simulated SER curve for 8PSK with perfect phase tracking and timing recovery coincides with the theoretical SER curve for 8PSK. Simulated SER curve with imperfect timing (but perfect phase tracking) shows a symbol SNR degradation of about 0.2 dB from the theoretical curve.

5. Discussion and conclusion

Current trends in mobile communications will be impacted from operational environment, many near-by users and spectrum sharing, expanding amounts of data (such as streaming video), and increased mobility of receivers. As such, there is higher potential to drop lock, and greater impact resulting from traditional recovery times. A proposed solution is to introduce RWF into the TRL to reduce drops, and also shorten reacquisition time. Based on the RWF-TRL simulation results for 8PSK comparing to standard TRLs for similar 8PSK modem, we believe that the proposed loop has the following advantages:

- Using adaptable threshold values of the RWF timing loop that is trained for specified operational environments, the "dropped lock" rate is expected to be less

- Faster acquisition time due to the adaptable threshold value setting of the RWF timing loop

- Can be made to be adaptive to any mobile environment using deep learning and artificial intelligent technology.

- All digital and simple to implement

- Expandable to accommodate a wide range of modulation schemes, namely, BPSK, QPSK, 16-QAM, 64-QAM, and possible application to continuous phase modulation, e.g., GMSK.

- The authors searched for similar SER results for 8PSK Modem to compare with the simulation results presented in Section 4.3, but currently, there are no TRL using RWF available for performance comparison.

As described in Section 4, there are several features associated with RWF approach, including:

- Operate at low sampling rate, which means less power consumption.

- Provide excellent SER performance

- Robust to mobile operational environment due to adaptable feature

- Accommodate a wide range of modulation schemes

The potential markets for the proposed RWF filter approach include:

- Mobile satellite industry: Mobile satellite terminals, satellite decoders, etc.

- Wireless communication industry: Cellular and mobile phone industry.

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Conflict of interest

Using the data reported in [1], which was performed under The Aerospace IRAD funding in early 2000's, the authors prepared Sections 2.4 and 4 of this chapter. However, the preparation of this chapter was not funded by The Aerospace Corporation, and it was done by the authors using their own time and thus it does not

represent The Aerospace Corporation's view on the use of RWF-TRL for future mobile satellite systems.

Notes/Thanks/Other declarations

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