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An Inductive-Coupling Inter-Chip Link for High-Performance and Low-Power 3D System Integration

Kiichi Niitsu and Tadahiro Kuroda
Keio University
Japan

1. Introduction

Three-dimensional (3D) system integration is one of the promising candidates for the next-generation high-performance and low-power LSI systems. In 3D system integration, we can implement analog and digital circuits in LSI chips in their optimal process and they are stacked and connected through vertical inter-chip link. Development of wide-band and low-power inter-chip link is the key factor to realize high-performance 3D system integration.

One of the most attractive applications of 3D system integration is processor-memory interface since memory capacity and bandwidth is a bottleneck of a processor system. Integrating large size memory on a processor increases die size (SRAM) or process steps (eDRAM), either way, raising cost and leakage. It is desired in low-power consumer electronics that a memory chip and a processor chip are each fabricated in their optimal process and integrated by heterogeneous chip stacking in a package. One of the technical challenges is a wide bandwidth between the processor and the memory. The gap between computing power and communication bandwidth can be filled if chip area is used for a data link rather than chip periphery only. A Micro-bump and a capacitive-coupling link (Fazzi et al., 2008) are area interfaces, but they can be used only for two chips that are placed face-to-face. A Through Silicon Via (TSV) (Koyanagi et al., 2009) has fewer limitations, but it requires additional process steps and production equipment. An inductive-coupling link (Miura et al., 2007) is used as a wireless TSV, but with small impact on cost. It is a circuit solution on a standard CMOS process, and hence is less expensive than TSV. It bears comparison with TSV in performance. The data rate is 11Gb/s/channel (Miura et al., 2009) and power efficiency is 65fJ/b (Niitsu et al., 2008). 1Tb/s aggregated bandwidth is achieved by arranging 1000 channels in 1mm^2 in 0.18μm CMOS, and BER is lower than 10^{-14} (Miura et al., 2007). Furthermore, it provides an AC-coupled interface, and therefore a level shifter is not needed. Power supply voltages can be different, and they can be changed for dynamic voltage scaling (DVS) and power gating with little impact on interface delay. An ESD protection device is not needed, either.

Figure 1 shows the concept of 3D system integration using an inductive-coupling link. Processor chips, memory chips and analog and RF front-end chips are implemented in each optimized process and stacked. In addition to data and clock, wireless inductive-coupling power delivery with high-frequency was demonstrated (Onizuka et al (2006)). By utilizing

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wireless inter-chip power delivery, we can omit conventional wire-bondings for power supply and achieve further cost reduction.

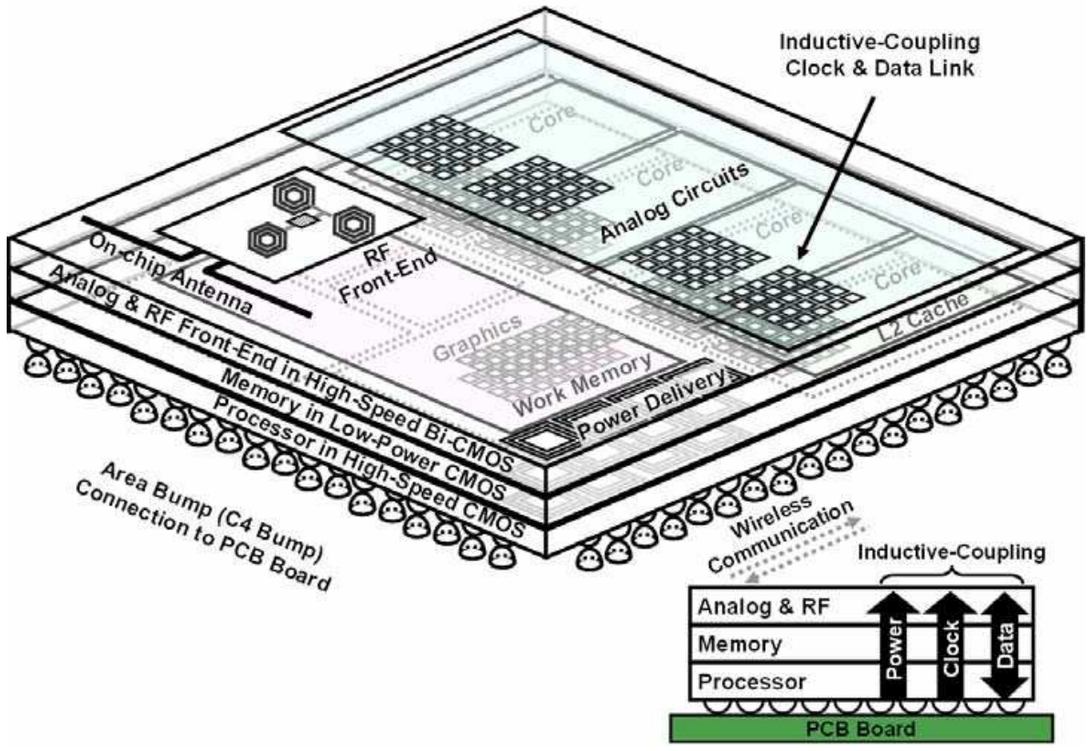

Fig. 1. 3D system integration using an inductive-coupling link.

This chapter is organized as follows. Section 2 introduces transceiver design of an inductive-coupling link. Section 3 reports the interference between an inductive-coupling link and other circuits. In Section 4, the modelling and experimental verification of tolerance to misalignment between stacked chips are introduced. In Section 5, application of an inductive-coupling link to processor-memory interface is shown. Section 6 concludes the chapter.

2. Inductive-coupling inter-chip link

Figure 2 shows the transceiver circuits for inductive-coupling inter-chip link. Bi-phase modulation is employed. Transmitter circuit consists of an H-bridge circuit which generates positive or negative pulse current, IT according to transmit data, Txdata. In every clock cycle, positive pulse is generated when Txdata is high, and negative pulse is generated when Txdata is low. In the receiver circuit, positive or negative pulse voltage, V_R that corresponds to the polarity of I_T is induced in the receiver inductor. Receiver circuit samples V_R, and then it recovers a binary receiver data, Rxdata. Since the complementary type latch is used as a sense amplifier, the receiver consumes power only at clock rising edge. Transmitter consumes power by I_T generation. Because of the weak coupling between transmitter inductors and receiver inductors, large pulse current I_T is necessary for generating enough V_R. Therefore, transmitter consumes higher power than receiver.

In our previous work (Miura et al., 2007), the transceiver consumes 3W at 1Tb/s. 80% of total power is consumed in transmitter. The power reduction of the transmitter is more critical in reducing the total power.

As explained above, an inductive-coupling link generates magnetic flux, which causes interference from/to other circuits. In Section 3, the investigation of this interference will be provided.

Besides, in order to achieve low-power operation, synchronous scheme is utilized in an inductive-coupling link. In Section 4, timing adjustment scheme is proposed and applied to processor-memory interface.

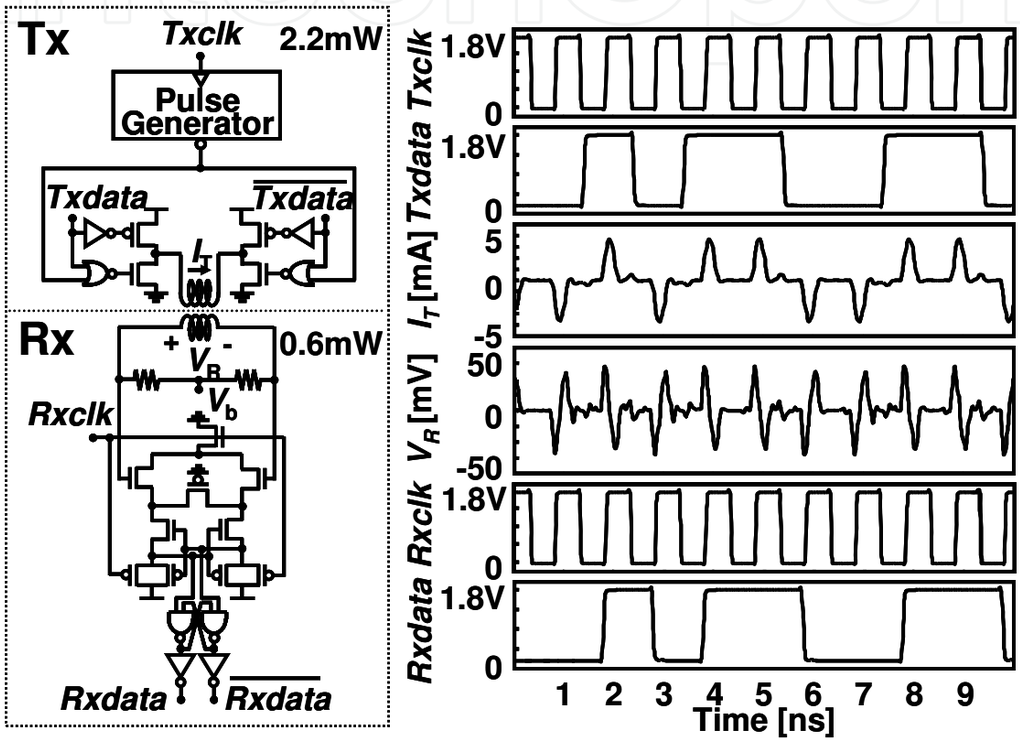

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Fig. 2. Transceiver circuits of an inductive-coupling link.

3. Interference of inductive-coupling link and other circuits

3.1 Introduction

In this section, interference from power/signal lines and to SRAM circuits of inductive-coupling link is discussed. This section is organized as follows. 3.2 and 3.3 describe the analyses and mitigation techniques of interference from power lines and signal lines, respectively. 3.4 describes the analysis and mitigation technique of interference to SRAM circuits.

3.2 Interference from power lines to an inductive-coupling link

In state-of-the-art LSI chips, the occupied area of power lines is increasing. However, power line degrades the performance of inductive-coupling link since eddy current in power line reduces magnetic flux as shown in Figure 3.

The shape of power line decides how much coupling degradation occurs. In this study, the dependence on the influence from the shape of power lines is compared. As the common power line, three types of power lines are investigated. Mesh type is employed in high-performance LSI chips such as microprocessor. The line and space type is employed for mobile application. The line and space type is classified into two types, without side line (type I) and with side line (type II). Type I has the loop of metal wire, while type II does not. Figure 4 shows the simulated trans impedance (the ratio of received voltage to the transmit current) at 1 GHz dependence on the metal density filled by the power lines.

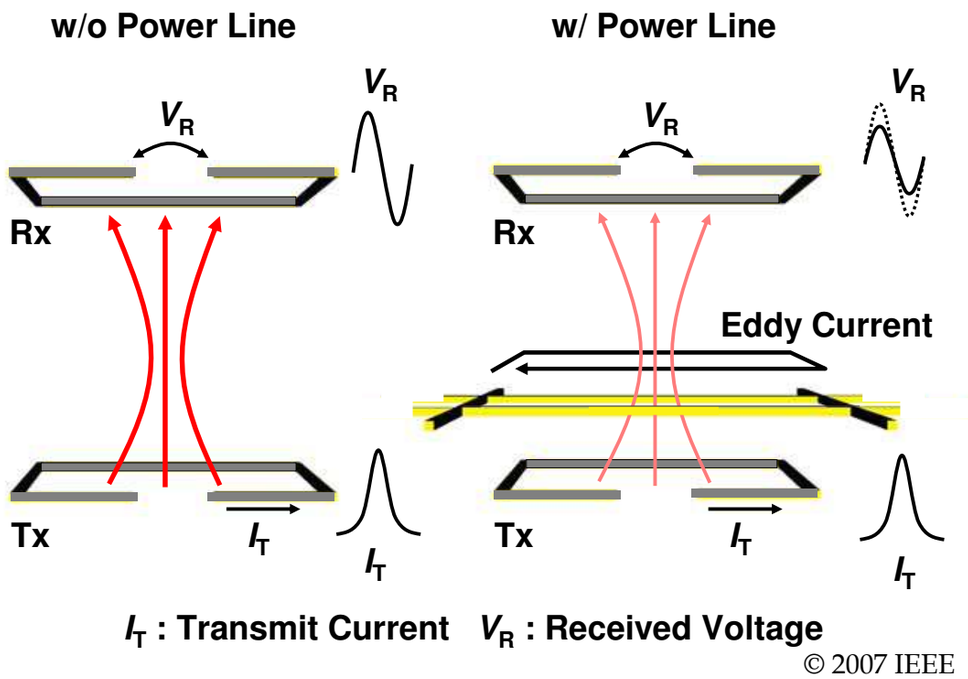

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Fig. 3. Coupling degradation by eddy current in power lines.

For this simulation, three-dimensional electromagnetic solver is employed. The thickness of metal layer and the gap of metal layer are set to 0.5 μm.

From simulation results in Fig. 4, it can be seen that the mesh type of power line (for high-performance LSI) affects the performance of inductive-coupling link more significantly than others. The line and space (I) does not reduce the transimpedance since there is no loop of metal wire and hence eddy current does not flow. The line and space (II) affects the inductive-coupling link more seriously than line and space(I). The influence by Line and space (II) does not change between 20% and 50%. The reason is that long side of metal wire is dominant when power line diminishes magnetic flux.

In order to measure the interference from power lines, test chips were designed and fabricated in 65nm CMOS. Figure 5 depicts microphotograph of stacked chips fabricated in this research. The area of this test chip is 3.5 mm * 2.5 mm and 2.5 mm * 1.9 mm. It consists of 20 types of transceivers with different configurations. The transmitters have an on-chip metal inductor whose outer diameter is 160 μm and 80 μm. As shown in Fig. 5, test chips are stacked face to back (both face-up) and communication distance is 70 μm. The upper chip was polished and its thickness is 50 μm. The thickness of adhesive layer is 20 μm. Probe card was utilized for this measurement.

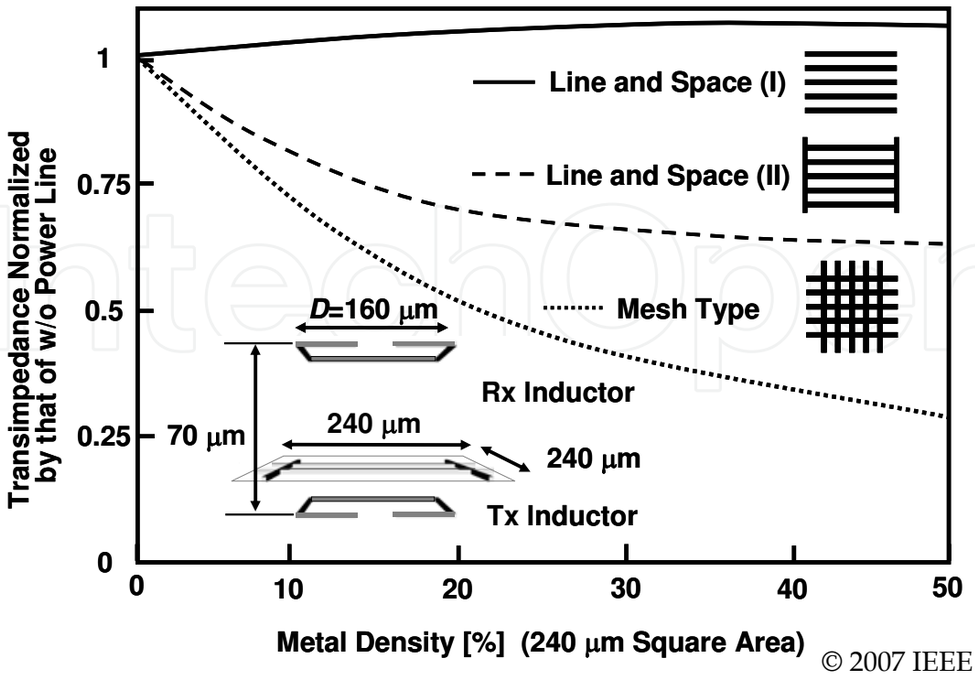

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Fig. 4. Simulated transimpedance dependence on type of power line.

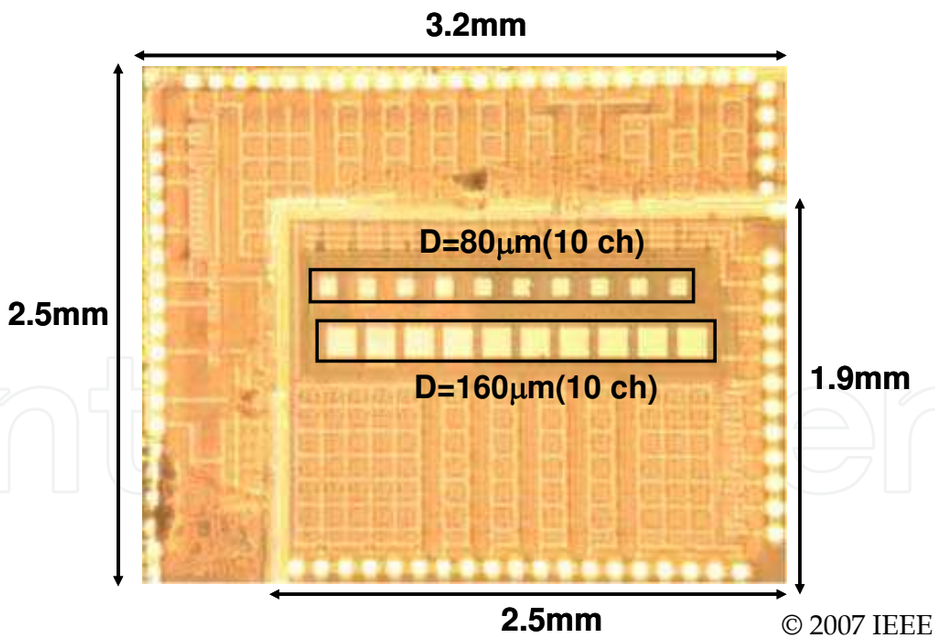

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Fig. 5. Stacked chip microphotograph.

Figure 6 shows measured transmit power dependence on metal density. Transmit power is measured when achieved bit error rate (BER) is same. In Fig. 6, vertical axis is normalized by transmit power when there are not power lines but dummy metals above the inductors. Measured result matches well with simulation result in the case of line and space (I) and (II).

However, measured result of mesh type of power line is less than simulation result. The accuracy may improve by taking eddy current in substrate into consideration.

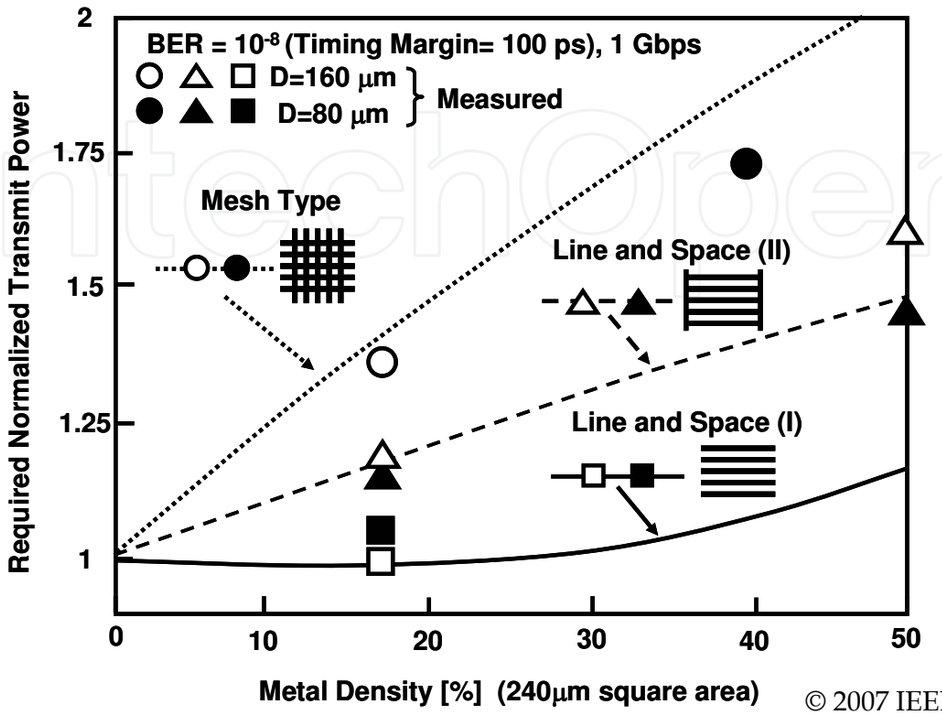

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Fig. 6. Measured transmit power dependence on types of power line.

3.2 Interference from signal lines to an inductive-coupling link

Immunity to interference from high-speed signal lines is a very important issue in the implementation of the inductive-coupling link with recent LSI chips. Especially, receiver circuits may not have high immunity to interference from high-speed signal line since receiver circuits sample very small signal. In this work, we implemented high-speed signal lines near transceiver inductors of the inductive-coupling link. With this implemented module, influence to the operation of inductive-coupling link when high-speed signal lines drive large capacitance is measured.

For the purpose of measuring the influence from signal lines, we implemented signal line under the inductive-coupling link. In previous work, mutual inductance between signal line and inductor dependence on the position is simulated. From simulation result, mutual inductance is maximized when the signal line is allocated under the center between the lines of inductor. In this study, 3 mm length signal line is implemented under the transceiver inductors. Near the inductors, buffer is implemented to drive signal line with 3 mA peak-to-peak.

Fig. 7 depicts measured BER dependence on the timing between driving signal line and sensing transmit current in the inductive-coupling link. Influence on the transmitter inductor is smaller compared with that on the receiver inductor. The disadvantage of placing high-speed signal line near the inductive-coupling link is as small as 9% additional transmitter power consumption.

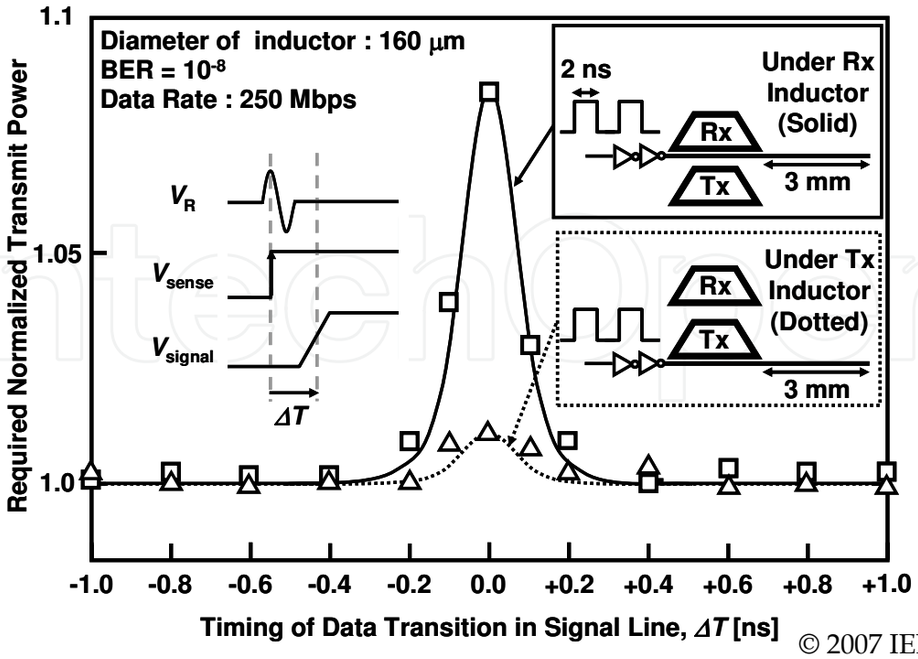

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Fig. 7. Measured required transmit power to achieve communication performance dependence on the timing of data signal.

Since power of an inductive-coupling link has become lower than other interfaces by developing low-power techniques such as in the previous work (Niitsu et al., 2008), 9% additional transmitter power can be neglected. In implementing inductive-coupling link near the logic circuits, precise care for timing between them is not necessary.

3.2 Interference from an inductive-coupling link to SRAM array operation

In order to develop high-performance LSI system, large-size of SRAM is necessary. Recently, the proportion of SRAM area to whole chip size is increasing rapidly (Hattori et al., 2006 & Ito et al., 2007). However, large on-chip SRAM causes yield degradation and increase of leakage power. As a solution of this problem, SRAM will be implemented in another chip, and three-dimensionally stacked. Inductive-coupling link will be utilized as an interface between SRAM and processor core. In this situation, magnetic flux from inductive-coupling link will be very important issue from the view point of reliable SRAM operation. In this study, electromagnetic interference on SRAM was measured and investigated.

At first, we estimated interference to SRAM circuits from inductive-coupling link in the case of 32 Kbit modules. Figure 8 illustrates the simple model of the inductive-coupling link and SRAM module.

The scattering parameter between transmitter inductor and bit line is extracted with three-dimensional electromagnetic solver. Figure 9 shows the bit-line noise induced by transmitter of inductive-coupling link. As shown in this waveform, the voltage of bit-line noise from inductive-coupling link is less than 1mV. In SRAM circuits such as (Yamaoka et al., 2005), even small voltage affects the performance such as operation speed and power dissipation. However, the sensing voltage is almost 50 mV, and the bit-line noise from inductive-coupling link is less than 1 mV. The bit-line noise from inductive-coupling link is very small compared with sensing voltage.

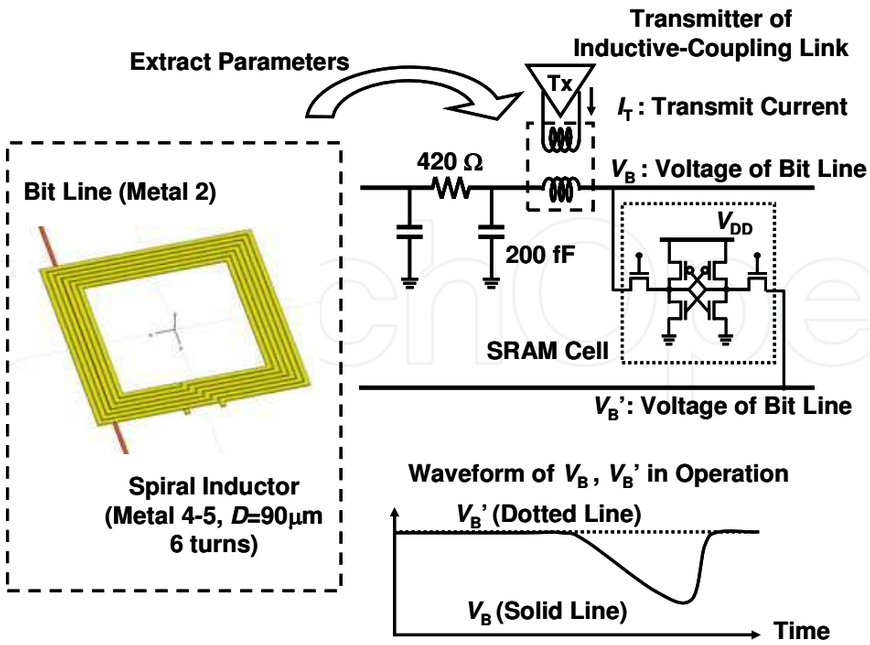

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Fig. 8. Simple model of inductive-coupling link and SRAM circuits.

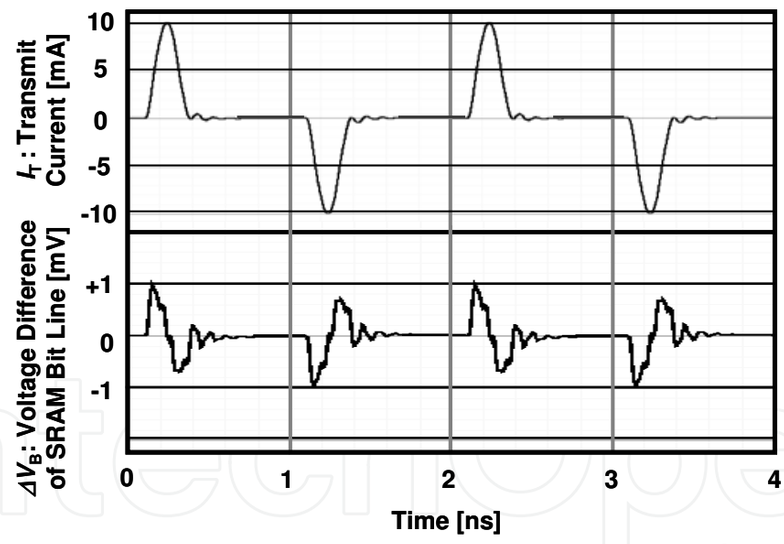

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Fig. 9. Simulated waveform of transmit current and voltage induced in SRAM bit line.

For the measurement to investigate influence to SRAM, another test chip was fabricated. This test chip was also fabricated in 65 nm CMOS. In this test chip, inductor with transmitter circuit was implemented above the SRAM arrays. SRAM circuits were allocated as Fig. 10 for influence on the bit line to be maximized.

Figure 11 depicts the measured waveform of output voltage. In this measurement, SRAM module repeated read and write toggle data pattern. As shown in Fig. 11, error occurs only when the inductive-coupling link generates transmit pulse current.

Figure 12 shows measured error rate in read operation of SRAM dependence on supply voltage. The difference of minimum supply voltage to maintain operational performance is only 10 mV when supply voltage is much lower than typical range. In typical region of SRAM operation, there is no difference between with the inductive-coupling link and without it. It is clear that influence on SRAM from inductive-coupling link is negligible. Influence from the inductive-coupling link is less serious than that from soft errors. That is why the inductive-coupling link does not affect SRAM operation in typical region of supply voltage while soft errors may affect. Compared with influence from device variations, it is much smaller since the difference in supply voltage of 10 mV corresponds to the difference in threshold voltage variation of 1 mV (Yamaoka et al., 2004), which is much smaller than process variation. From this measurement result, we have reached to a conclusion that inductive-coupling link can be placed near the SRAM circuits.

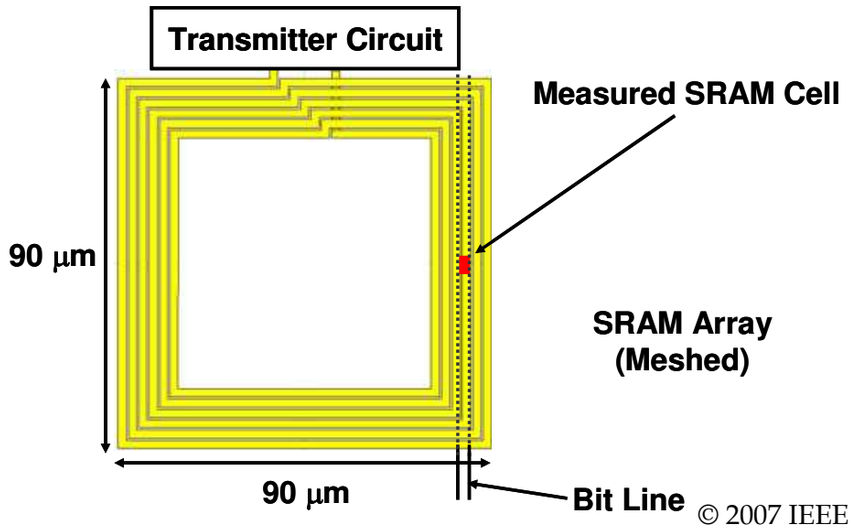

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Fig. 10. Test element group to measure the influence to SRAM circuits.

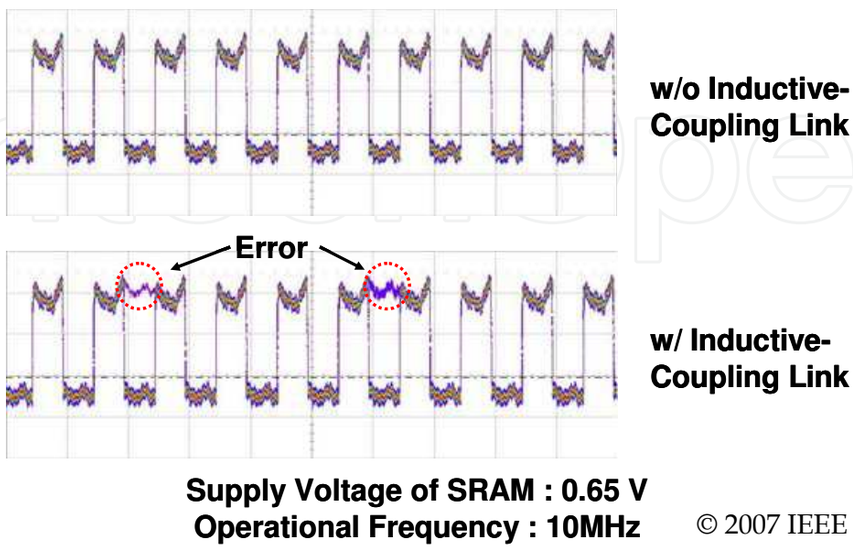

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Fig. 11. Measured waveform.

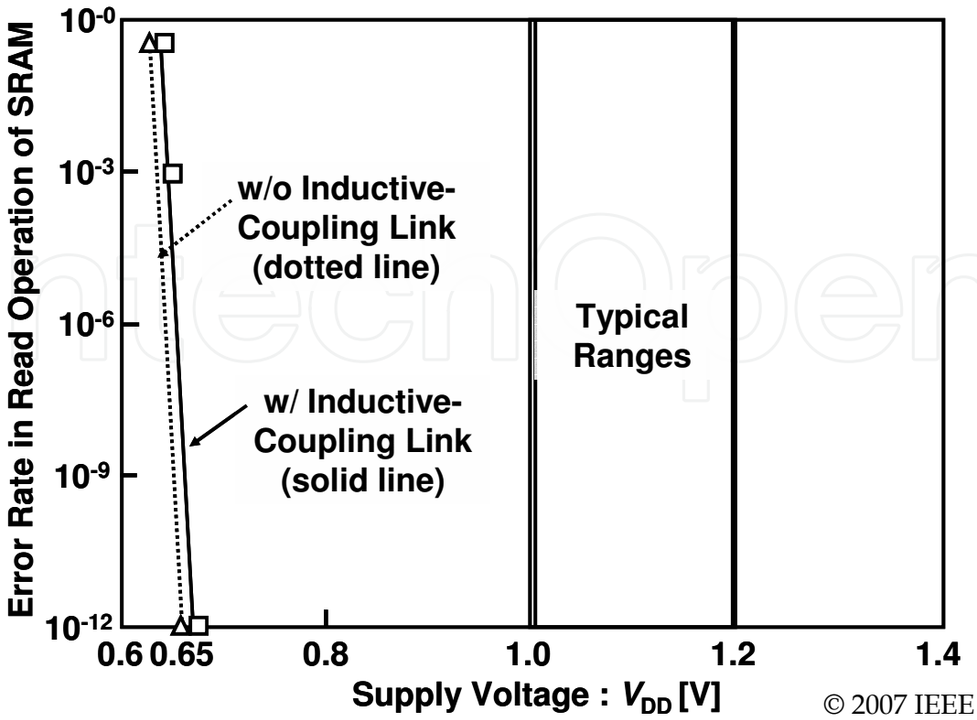

Fig. 12. Error rate in read operation dependence on supply voltage of SRAM circuits.

4. Misalignment tolerance of inductive-coupling link

4.1 Introduction

This section introduces modelling and investigation of misalignment tolerance of an inductive-coupling link. Figure 13 shows the conceptual image of increase in transmitter power due to misalignment between stacked chips. Because of misalignment, magnetic flux generated by the transmitter inductor can not be transferred to the receiver inductor. As a result, received voltage is attenuated. To keep received voltage constant under the misalignment, transmitter current must be increased and it causes increase in transmitter power. We proposed a model for estimating increased transmitter power due to misalignment.

4.2 Modeling of attenuation of received voltage

For the purpose of simplifying the analysis, self inductances of transmitter and receiver inductors are kept constant, same as that in magnetic field scaling (Mizoguchi et al., 2007?). This is achieved by adjusting the number of turns depending on the inductor's diameter. Pulse width is also kept constant for the timing margin to be constant. Under those conditions, received voltage is proportional to the coupling coefficient only (Finkenzeller, 2003).

Coupling coefficient, which is determined by communication distance and diameter of transceiver inductors, is reduced by misalignment since it increases communication distance equivalently as shown in Fig. 14. In order to compensate this reduction, transmitter power (here after, energy, which is normalized by data rate, for example, 1mW/1Gbps=1pJ/b) should be increased. Normalized required transmitter energy (E'/E) can be approximated as below.

$$E'/E = \frac{1}{\left\{1+(2Z/D)^2\right\}^{\frac{3}{2}}} \Bigg/ \frac{1}{\left\{1+(2Z'/D)^2\right\}^{\frac{3}{2}}} = \left\{\frac{D^2+4(Z^2+\Delta X^2+\Delta Y^2)}{D^2+4Z^2}\right\}^{\frac{3}{2}} \quad \because Z' = \sqrt{Z^2+\Delta X^2+\Delta Y^2} \tag{1}$$

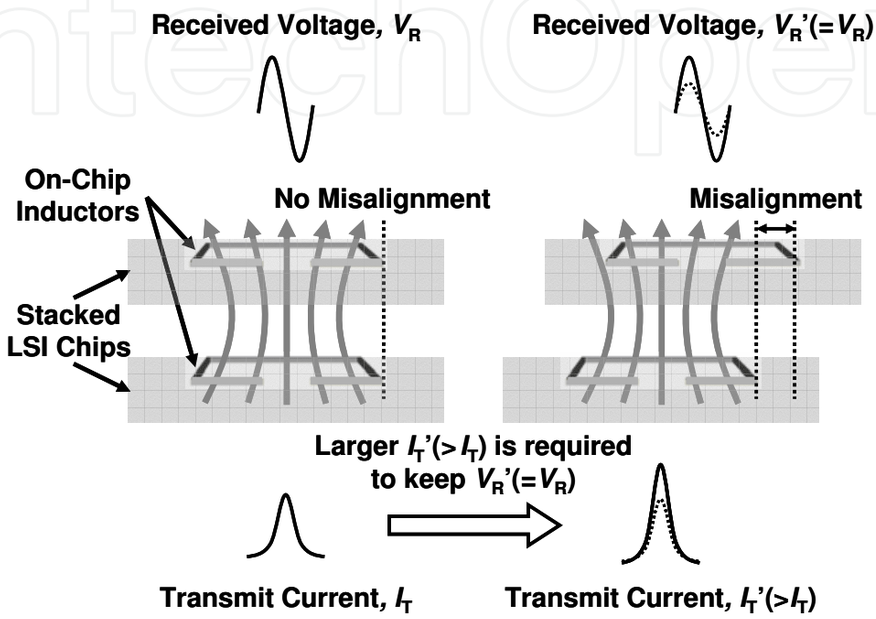

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Fig. 13. Concept of increase of transmitter power due to chip-to-chip misalignment.

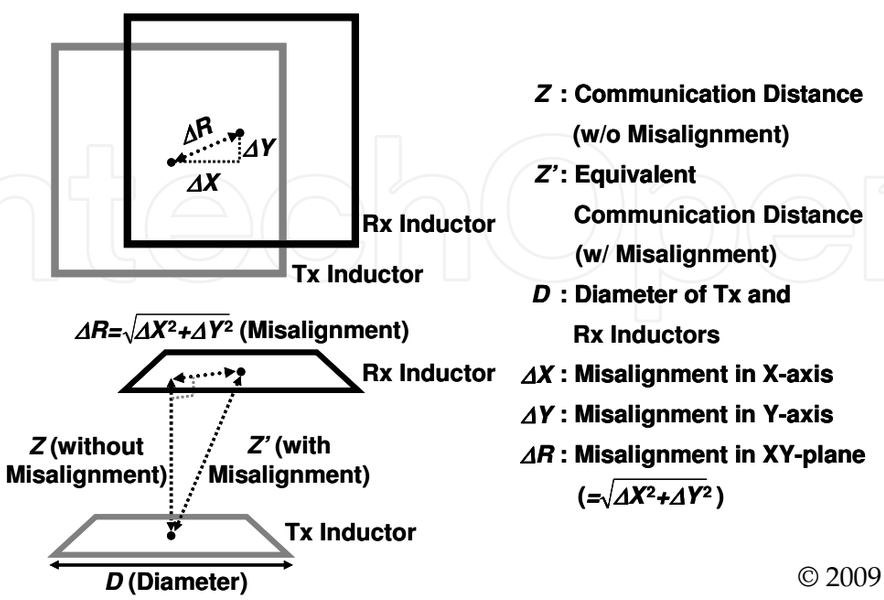

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Fig. 14. Increase of communication distance due to misalignment.

Where, E′ and E are the transmitter energies in case of with and without misalignment, respectively. Z′ and Z are the equivalent communication distances with and without misalignment, respectively. D is the average between outer and inner diameter of inductors. ΔX and ΔY are the values of misalignment in X-axis and Y-axis, respectively.
Figure 15 shows the total transmitter energy dependence on the angle of the inductor where the misalignment value, ΔR is constant. The diameter and communication distance are 80μm and 70μm. respectively. As shown in this figure, the difference of transmitter energy for all angles is less than 5%. This result shows that proposed modeling can be applied to not only 1D analysis but also 2D analysis.

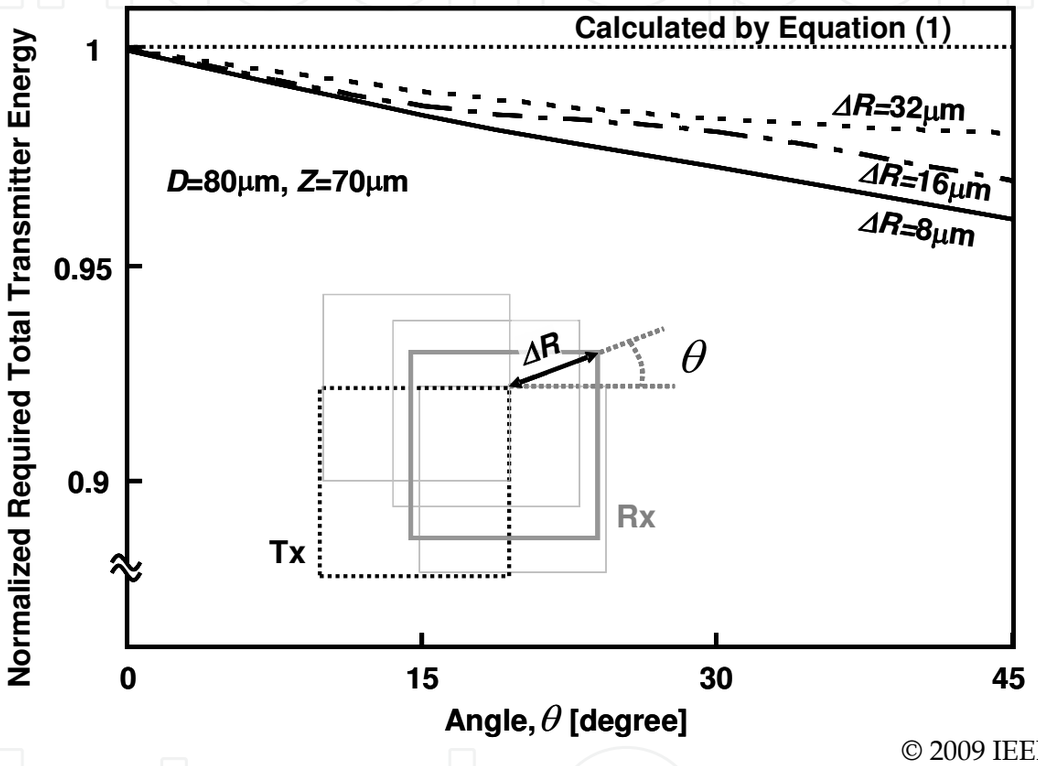

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Fig. 15. Normalized total transmitter energy dependence the position of the inductor.

4.2 Estimation of transmitter energy under misalignment

From the above theoretical analysis, we can calculate the relationship between design parameters and misalignment, which is shown in Fig. 16. By referring to this figure, parameter design with taking misalignment into consideration becomes possible. In order to determine the specific value of transmitter energy, we targeted the BER and timing margin. However, the proposed model can be applied to any BER and timing margin by scaling the transmitter energy calculated by (1). The reason is that misalignment affects only coupling coefficiency and the relationship between BER, timing margin, transmitter energy and coupling coefficient is introduced in (Miura et al., 2007). In Fig. 16, the region where (1) is valid will be explained in the following discussion. As shown in Fig. 16, there are points where magnetic filed lines change the vertical direction. If the directions of all magnetic field lines in the receiver inductor are same, (1) is valid. Such points were calculated from the

simulation by 3D electro-magnetic (EM) solver and plotted in Fig. 16. When Z/ΔX is more than approximately 0.8, (1) gives accurate value and its accuracy is confirmed by comparing with simulation results by EM solver and measurement results in the following sections.

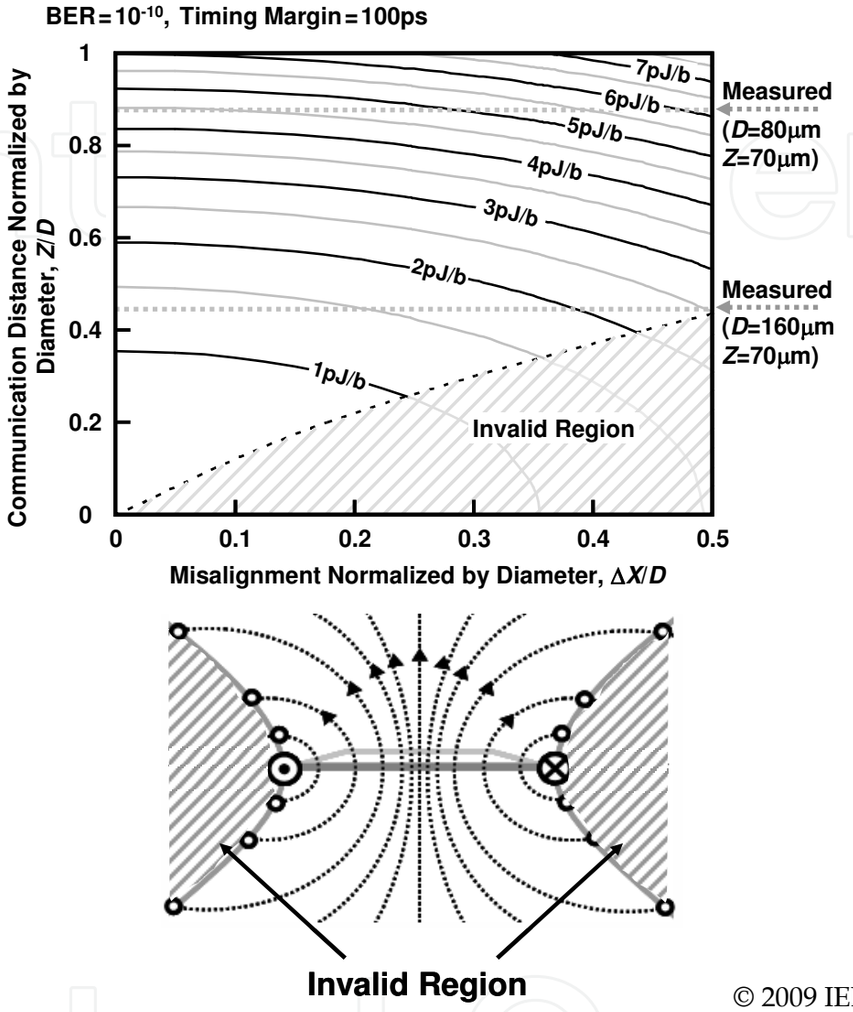

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Fig. 16. Relationship among energy dissipation, normalized misalignment and communication distance.

4.3 Estimation of transmitter energy with consideration of crosstalk

Misalignment also affects the performance in array operation. In arrayed inductive-coupling link, bit error rate is given by the following equation (Miura et al., 2007).

$$\mathrm{BER} = \frac{1}{2}\mathrm{erfc}\left(\frac{\tau}{4\sqrt{2}\tau_{j,rms}}\sqrt{\ln\frac{S-\mathrm{C}-\mathrm{N}}{\mathrm{N}}}\right) \tag{2}$$

Note that erfc() is the error faction complement, τ is the pulse width of transmitter current, $\tau_{j,rms}$ is rms jitter of sampling clock in receiver, S is signal, N is ambient noise and C is crosstalk.

As in (2), in order to keep the same BER, the difference of signal(S) and crosstalk(C), has to be maintained. The value of ambient noise, N, is constant in both cases with and without misalignment. Since signal is attenuated and crosstalk is increased due to misalignment (Fig. 17), transmitter energy needs to be increased to maintain that difference.

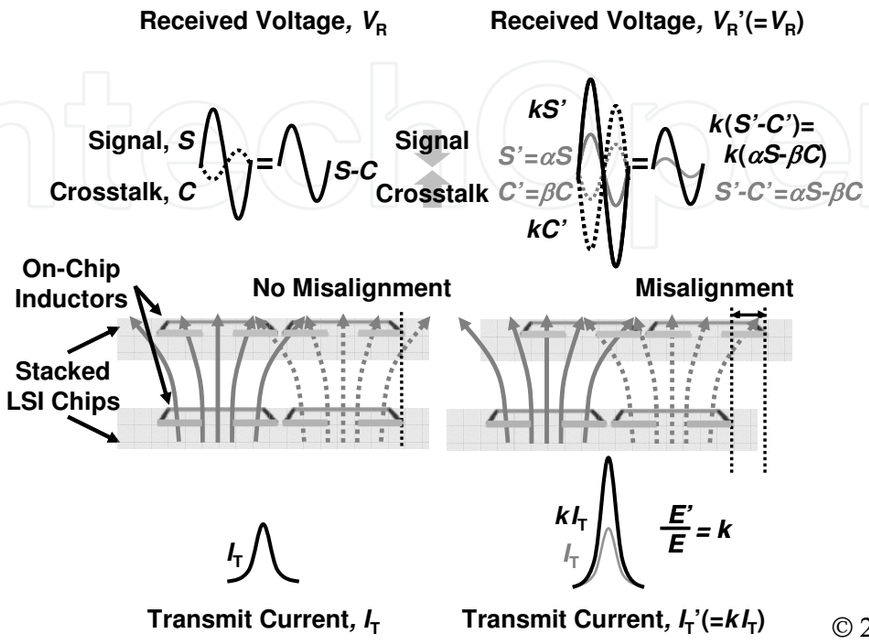

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Fig. 17. Increase of crosstalk due to misalignment.

In order to estimate the transmitter energy with consideration of misalignment in array operation, we propose the simplified model. At first, crosstalk is assumed to be proportional to $1/R^3$ as reported in (Miura et al., 2004), where R is horizontal distance from the channel which causes crosstalk. The values of crosstalk from Tx1 and Tx2 have already been known to be C_1 and C_2 since they are essential for estimating transmitter energy even without consideration of misalignment (Fig. 18). With these values, we can get the relationship between crosstalk, C and horizontal distance, R, and then, between required transmitter energy and misalignment as in the following equations.

$$\begin{cases} C_1 = A\dfrac{1}{{R_1}^3} + B \\ C_2 = A\dfrac{1}{{R_2}^3} + B \end{cases} \Leftrightarrow \begin{cases} A = \dfrac{C_1 - C_2}{\dfrac{1}{{R_1}^3} - \dfrac{1}{{R_2}^3}} \\ B = C_1 - A\dfrac{1}{{R_1}^3} \end{cases} \tag{3}$$

$$C_i = A\frac{1}{{R_i}^3} + B, \quad C_i' = A\frac{1}{{R_i'}^3} + B \tag{4}$$

Where, C'_i and C_i are crosstalk from i-th transmitter channel with and without misalignment, respectively. R'_i and R_i are horizontal distances from i-th transmitter channel with and without misalignment, respectively. A, B is the constant.

Signal attenuation due to misalignment is modeled by (1) as explained previously. With the above conditions, required transmitter energy can be approximated as bellow.

$$E'/E = k = \frac{S-\mathrm{C}}{S'-\mathrm{C}'} = \frac{S-\mathrm{C}}{\alpha S - \beta \mathrm{C}}$$

$$where \ \alpha = \left\{ \frac{D^2 + 4(Z^2 + \Delta X^2 + \Delta Y^2)}{D^2 + 4Z^2} \right\}^{-\frac{3}{2}}, \quad \beta = \frac{\sum_{i=1\sim 8} C_i'}{\sum_{i=1\sim 8} C_i} \tag{5}$$

Where, E′ and E are required transmitter energy with and without misalignment, respectively. α is the ratio of signal in the misaligned case to the signal in case with no misalignment, and β is the ratio of total crosstalk in 3×3 array between with and without misalignment as shown in Fig. 17.

Figures 18, 19 and 20 show the simulation condition, the absolute and normalized transmitter energy dependence on misalignment. The dependency on the angle is negligibly small and we investigated required transmitter energy with 1-D misalignment (X-Axis). Due to the increase in crosstalk, required transmitter energy for the same BER is increased. The gap between simulation results and calculation results by (5) is also increased.

In array operation, misalignment has to be taken into account more carefully especially when the channel pitch, P is small. Nevertheless, in usual conditions (D=80 μm, Z=70 μm, ΔX=16 μm, P=160 μm), increase in crosstalk due to misalignment is small enough to be ignored. A misalignment of 16 μm is found in commercial mass production.

From the above theoretical analysis, we can calculate the relationship between design parameters and misalignment, which is shown in Fig. 6.

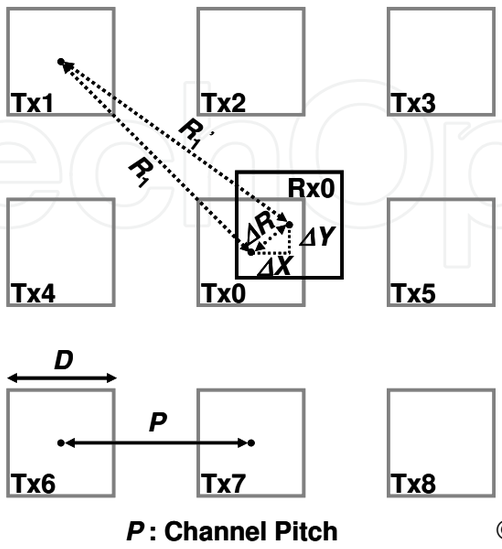

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Fig. 18. Simulation condition.

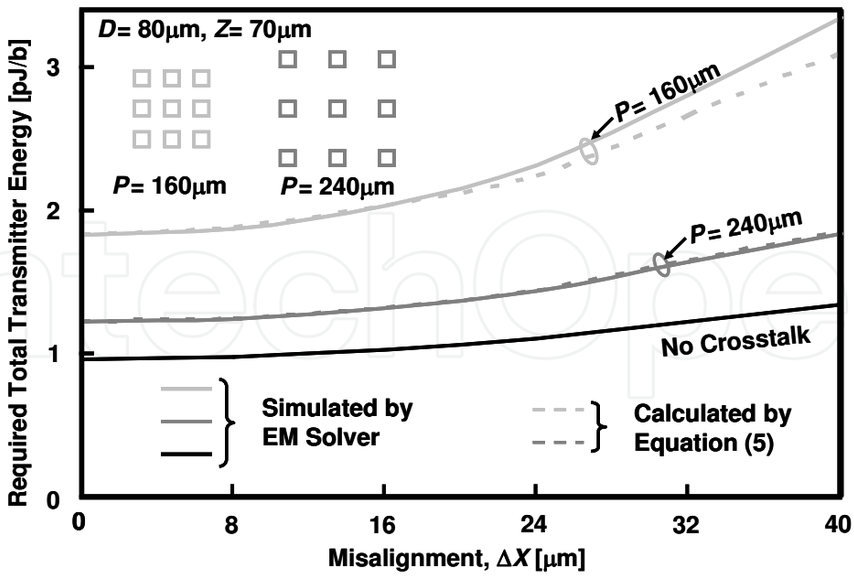

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Fig. 19. Required total transmitter energy dependence on misalignment in array operation.

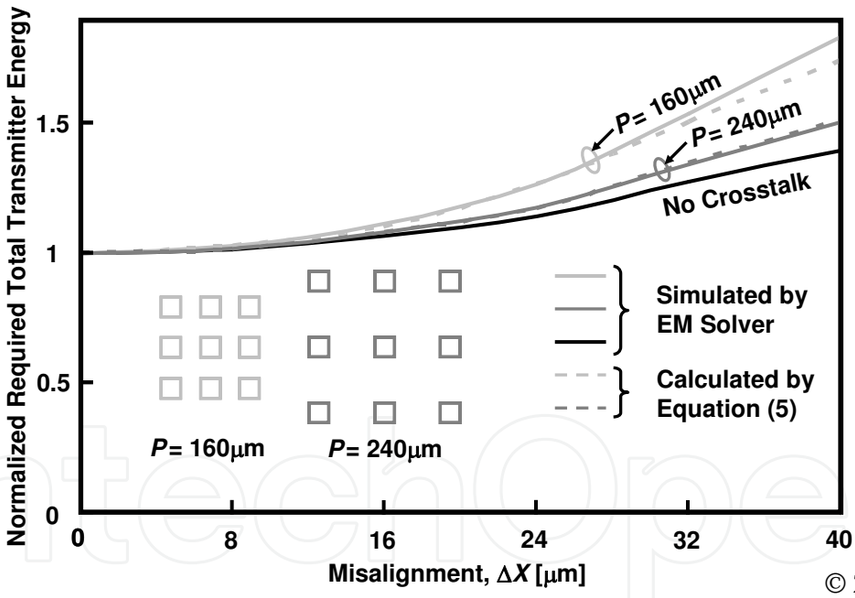

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Fig. 20. Normalized required total transmitter energy dependence on misalignment in array operation.

4.3 Experimental verification

Test chips shown in Fig. 5 were utilized for measurement. Figure 21 illustrates the test chip configuration. The transmitter and receiver chips have twelve channels. Transmitter inductors and receiver inductors are arranged with different pitches to make a misalignment. The difference of pitches in larger inductors (D=160 μm) and smaller inductors (D=80 μm) are 16 μm and 8 μm, respectively. With this configuration,

misalignments corresponding to 10%, 20%, 30%, 40%, 50% of the outer diameters of inductors are made.

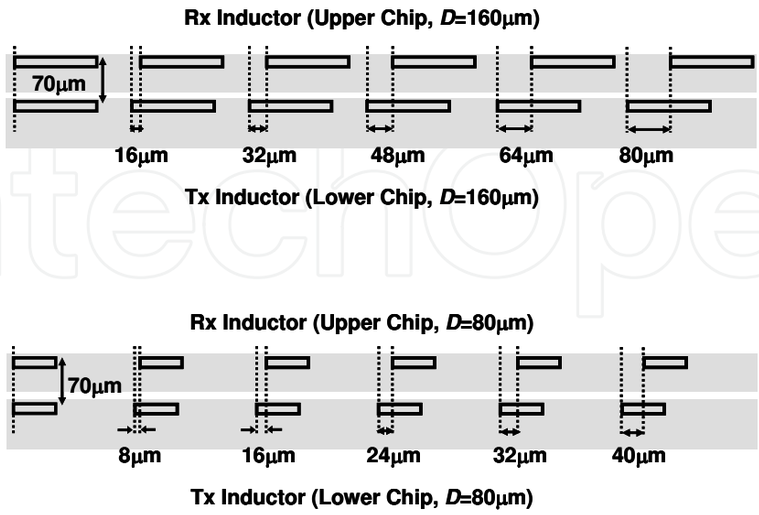

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Fig. 21. Test chip configuration.

Figures 22 and 23 show the absolute and normalized measured and simulated transmitter power dependence on the misalignment. In simulation, 3D electro-magnetic solver was used. The power dissipation in this figure is normalized by that without misalignment.

In usual condition (D=80 μm, Z=70 μm), 16 μm of misalignment, while ±10 μm is available in commercial mass production, can be compensated with increasing transmitter power by only 6%. It means that misalignment tolerance of inductive-coupling inter-chip link is high enough. Besides, influence of misalignment is less serious than that of process variations. On the other hand, through-Si via (TSV) technology requires alignment accuracy of ±1 μm (Matsumoto et al., 1998).

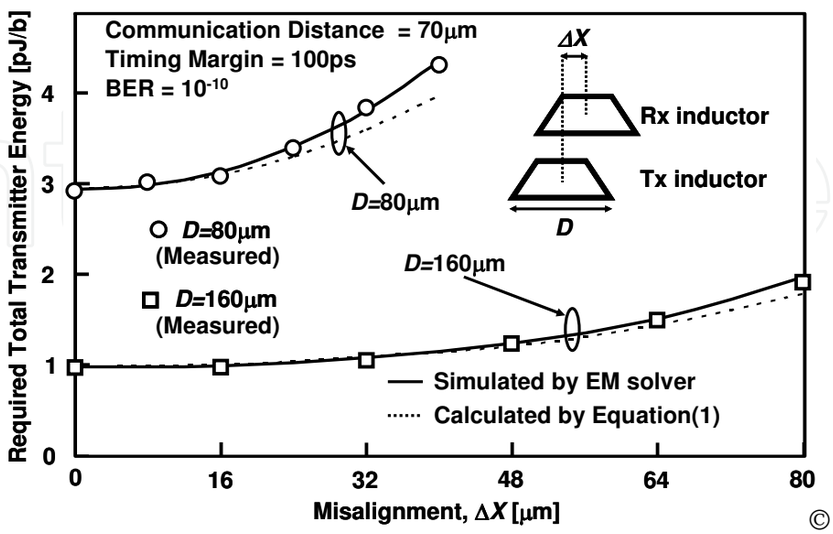

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Fig. 22. Measured, simulated and calculated total transmitter energy dependence on the value of misalignment.

Measured results match well with both simulation results from electro-magnetic solver and calculated results from (1). As mentioned in Sect. II, (1) does not cover all of region and has an invalid region. The gap between measured and calculated results becomes larger as the result curves approach the invalid region.

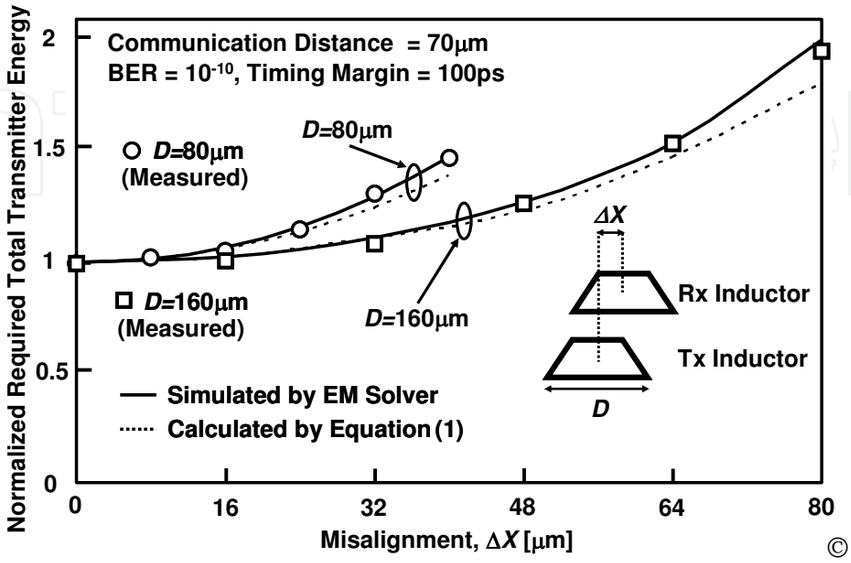

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Fig. 23. Measured, simulated and calculated normalized total transmitter energy dependence on the value of misalignment.

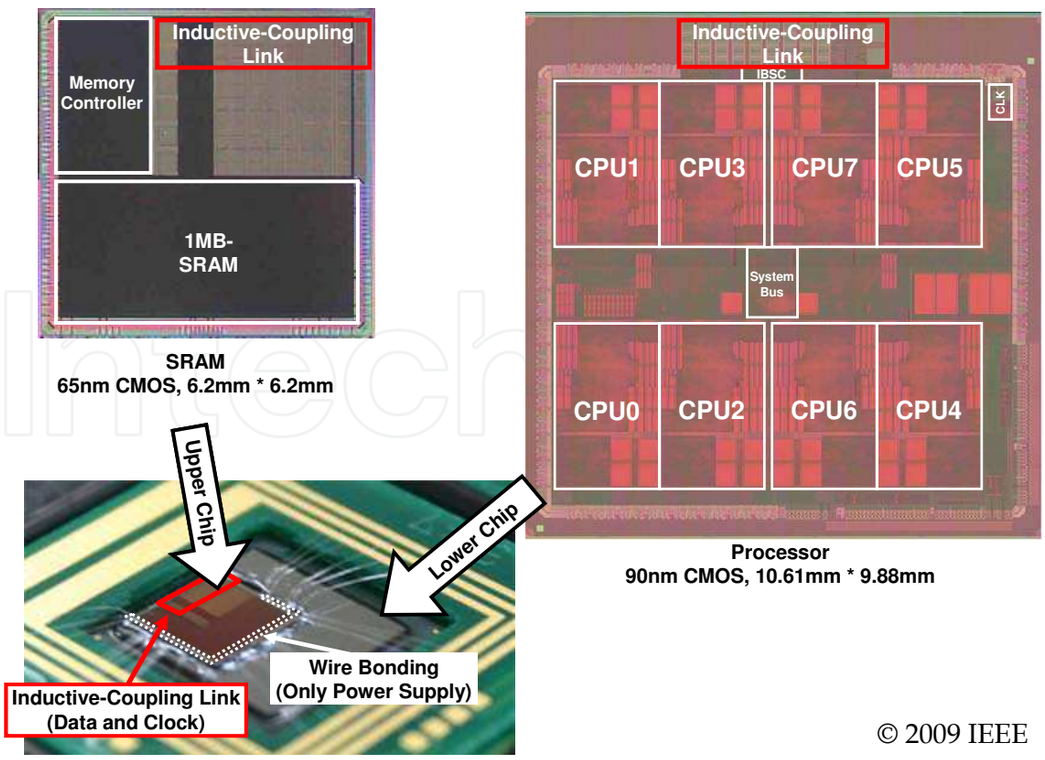

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Fig. 24. Chip microphotograph and overhead view of stacked chips.

5. Inductive-coupling link for processor-memory interface

5.1 Introduction

This section presents a three-dimensional (3D) system integration of a commercial processor and a memory by using inductive coupling. A 90nm CMOS 8-core processor, back-grinded to a thickness of 50μm, is mounted face down on a package by C4 bump. A 65nm CMOS 1MB SRAM of the same thickness is glued on it face up, and the power is provided by conventional wire-bonding. The two chips under different supply voltages are AC-coupled by inductive coupling that provides a 19.2Gb/s data link. Measured power and area efficiency of the link is 1pJ/b and 0.15mm²/Gbps, which is 1/30 and 1/3 in comparison with the conventional DDR2 interface respectively (Ito et al., 2008). The power efficiency is improved by narrowing a transmission data pulse to 180ps. Reduced timing margin for sampling the narrow pulse, on the other hand, is compensated against timing skews due to layout and PVT variation by a proposed 2-step timing adjustment using an SRAM through mode. All the bits of the SRAM is successfully accessed with no bit error under changes of supply voltages (±5%) and temperature (25°C, 55°C).

5.2 Performance summary of developed 3D LSI system

Micrographs of the chips and their stacking are presented in Fig. 24. A 90nm CMOS processor is mounted face down on a package by C4 bump. A 65nm CMOS SRAM is glued on it face up, and the power is provided by conventional wire-bonding.

Figure 25 summarizes performance. The two chips are each fabricated in their optimal process and supplied with optimal voltages. Thickness of the chips is both 50μm. The radius of the inductors is the same as the communication distance, 120μm. There are 18 data channels for uplink and downlink each. In total 36 inductors are arranged in a 243μm by 320μm pitch. Both the rising and falling edges of a clock are used for 2 phase interleaving to reduce crosstalk between the adjacent channels (Miura et al., 2007). There are clock channels for source synchronous transmission (Miura et al., 2009). One size larger inductors are employed to strengthen the coupling coefficient for asynchronous channel. Total layout area for the inductive coupling link is 2.82mm². Aggregated bandwidth is 19.2Gb/s. Area normalized by bandwidth is 0.15mm²/Gbps, which is 1/3 of a conventional DDR2 interface in the same technology (Ito et al., 2008). Since the previous designs of the processor and the memory were reused in large part, the inductive coupling channels are placed in the peripheral region. They can be distributed to each core if a chip layout is carried out from scratch. The circuitry alone occupies an area of 0.072mm², which is only 2.6% of the total area for the inductive coupling link. The area efficiency of circuit alone is therefore 0.0038mm²/Gbps, which is 1/120 of the conventional DDR2 interface. Even if the inductor is placed above a bit line of an SRAM and transmits data, no interference is observed (Niitsu et al., 2007). The inductive coupling can be applied to DRAM as well. The inductor can be constructed using 2 metal layers.

5.2 System architecture design with adaptive timing adjustment

Figure 26 depicts a block diagram of the developed 3D LSI system. An inductive-coupling bus state controller (IBSC) supports packet-based communications by adding two signals (vld and eop). A control register in IBSC is used for timing adjustment. The timing

Chip	Processor	SRAM
Process (Property)	90nm CMOS (High Speed)	65nm CMOS (Low Power)
Supply Voltage	1.0 V	1.2 V
Stacking	Face-Down	Face-Up
Connection with PCB	Area Bump	Wire Bonding
Thickness	50 μm	50 μm
Data and Clock Link	Inductive-Coupling	
Communication Distance	120μm (Glue:20μm)	
Inductor Size	Data : 240μm, Clock : 350μm	
Channel Pitch	X: 243μm, Y: 320μm	
Total Bandwidth	19.2 Gbps	
Energy Efficiency	1pJ/b (1/30 of DDR2)	
Area Efficiency	0.15mm²/Gbps (1/3 of DDR2)	

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Fig. 25. Performance Summary.

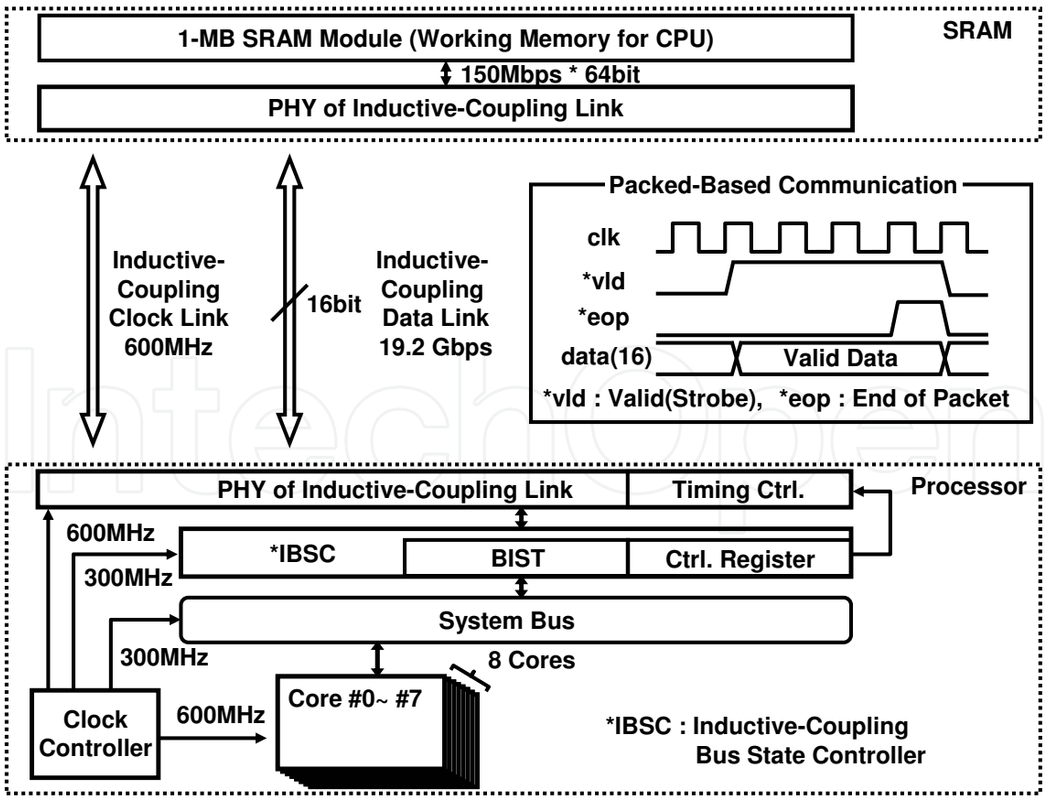

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Fig. 26. Block diagram.

adjustment is essential for a practical application. There is a trade off between power dissipation and timing margin. Since power dissipation in a transmitter is in proportion to the square of the pulse width (Miura et al., 2008), the narrower the pulse, the smaller the power dissipation. The timing margin for sampling the narrow pulse, however, will be reduced. Low-power design requires accurate timing control.

Adaptive circuits and systems are required to adjust the timing for the following reasons: 1) timing jitter caused by PVT variations, especially in a clock path with long latency through another chip, 2) VDD changes by DVS, and 3) inter-channel skews, especially when the channels are distributed in a wide area. The timing jitter under PVT variations can be monitored and calibrated by a coarse timing control unit with the control register in IBSC (Fig. 27). Once the calibration result under each condition of DVS is stored in the control register, the timing control unit can adjust the timing for DVS instantly by digital control.

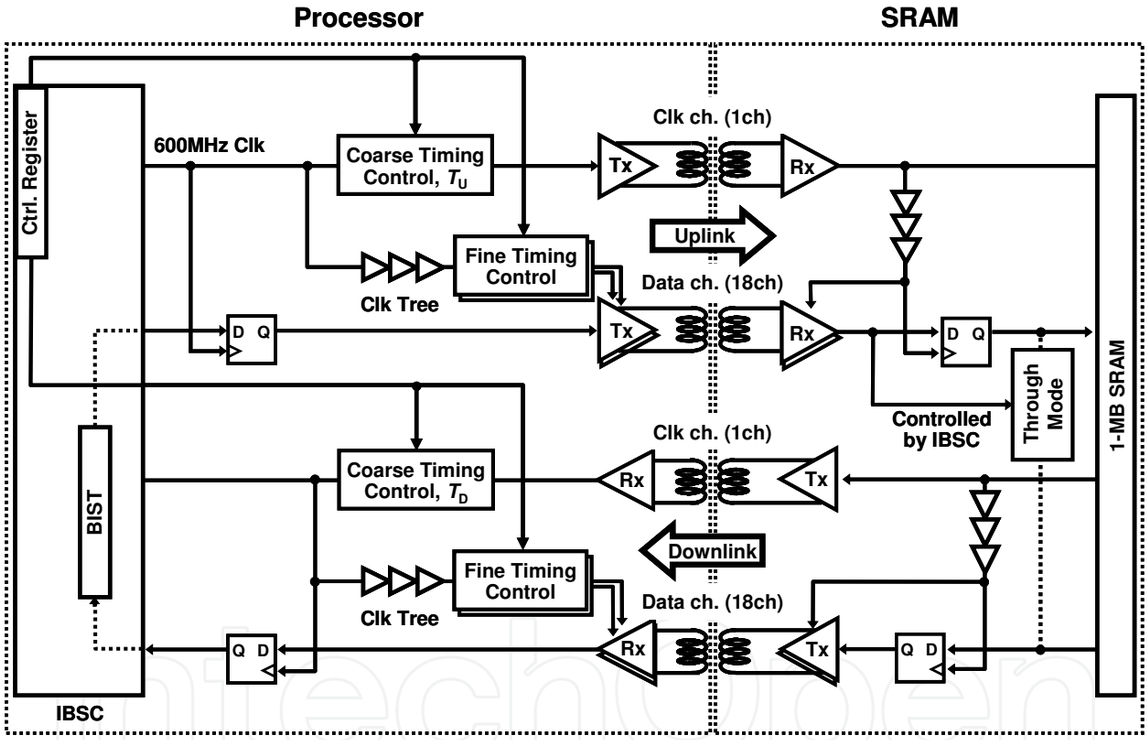

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Fig. 27. Adaptive timing adjustment.

The inter-channel de-skew can be performed by a fine timing control unit that is implemented in each channel. Figure 28 shows the timing adjustment flow that is controlled by the processor. First, the control register sets a loopback path in the SRAM for a test mode (an SRAM through mode). Secondly, pass/fail information, much like a shmoo plot, is stored in a register for both the uplink and downlink by changing the coarse timing. Thirdly, the coarse timing is set such that the timing margin becomes the largest when all the channels pass. For each channel, fine timing is tuned next such that the timing margin becomes the largest.

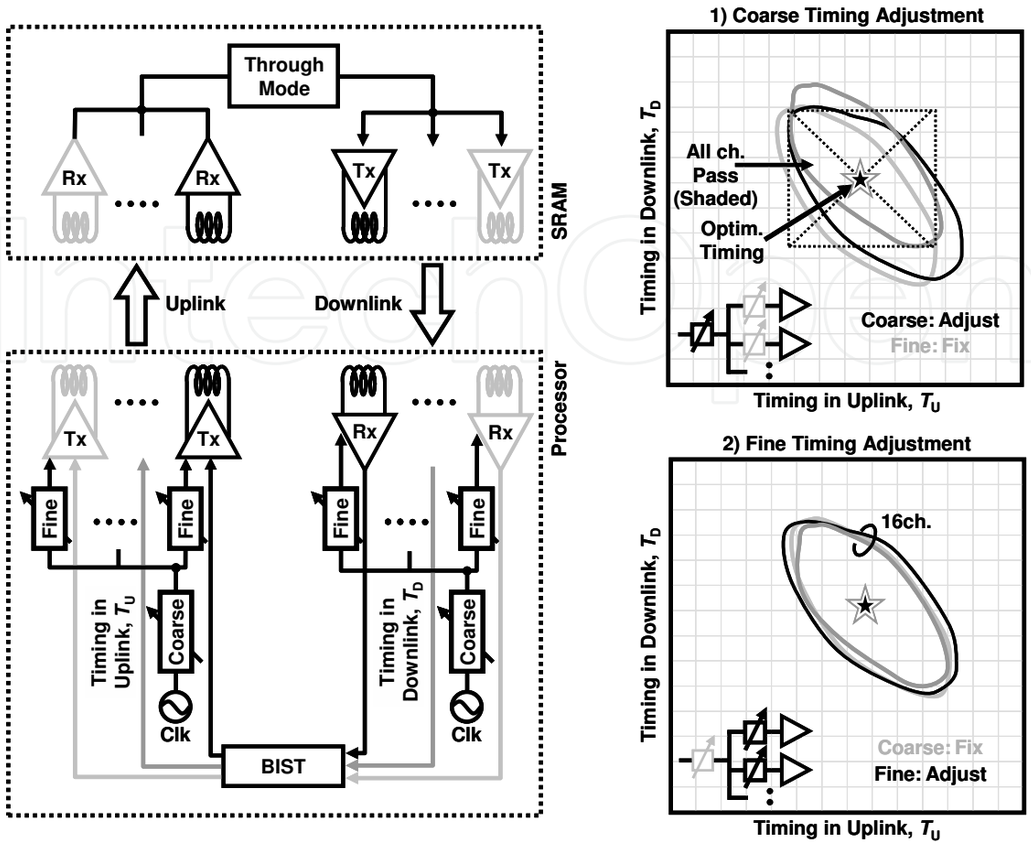

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Fig. 28. Fine and coarse (2-step) timing adjustment.

5.4 Measurement results and discussions

The SRAM was accessed (read and write) from the processor and BER was measured by changing the control register. A timing shmoo plot is depicted in Fig. 29, a bathtub curve marked by a broken line is also depicted. A BER of lower than 10^{-14} is achieved with a 2^{31}-1 PRBS. After optimizing the timing by setting the control register at the center of the shmoo plot, tolerance against VDD and temperature changes was measured. The measured result is presented in Fig. 30. No single bit failed under ±5% VDD variations and temperature ranges from 25°C to 55°C. The VDD tolerance can be improved from ±5% to ±10% by widening the pulse width from 180ps to 320ps at a cost of an increase in power efficiency from 1pJ/b to 2.5pJ/b (still 1/12 of DDR2).

6. Conclusion

This chapter presents the fundamental investigation and application of an inductive-coupling link.

First, the interference from power/signal lines and to SRAM of an inductive-coupling link was investigated. Measurement result shows that influence from line and space (I) is none and required normalized transmit power is 1.10 (line and space, type II) and 1.27 (mesh type) when metal density is 16%. The line and space type of power line is better for the

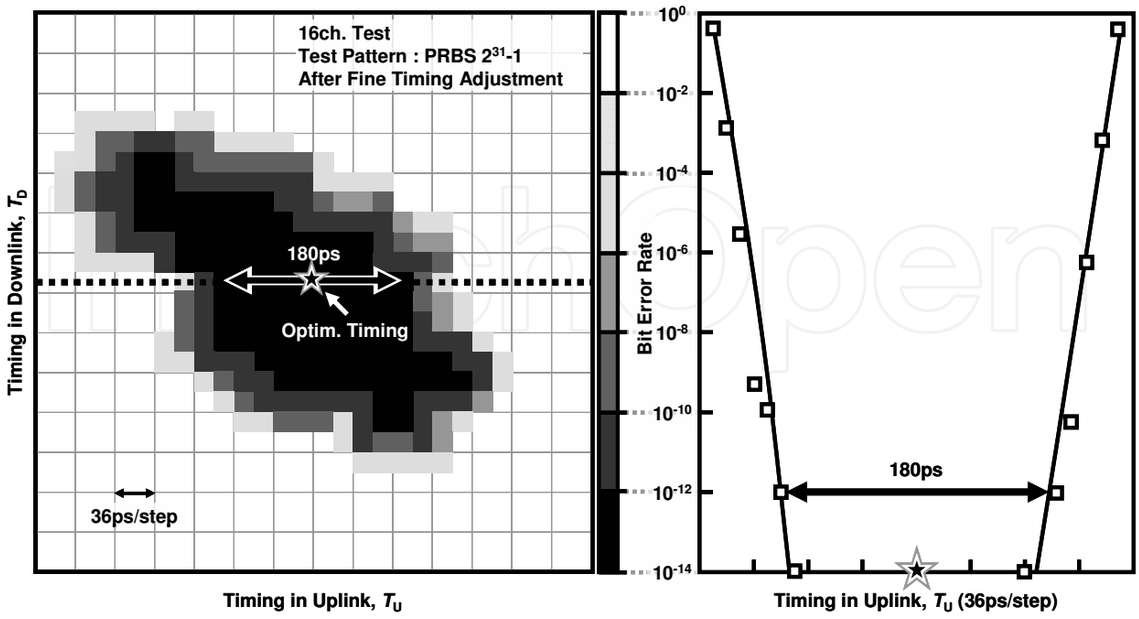

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Fig. 29. Measured bit error rate.

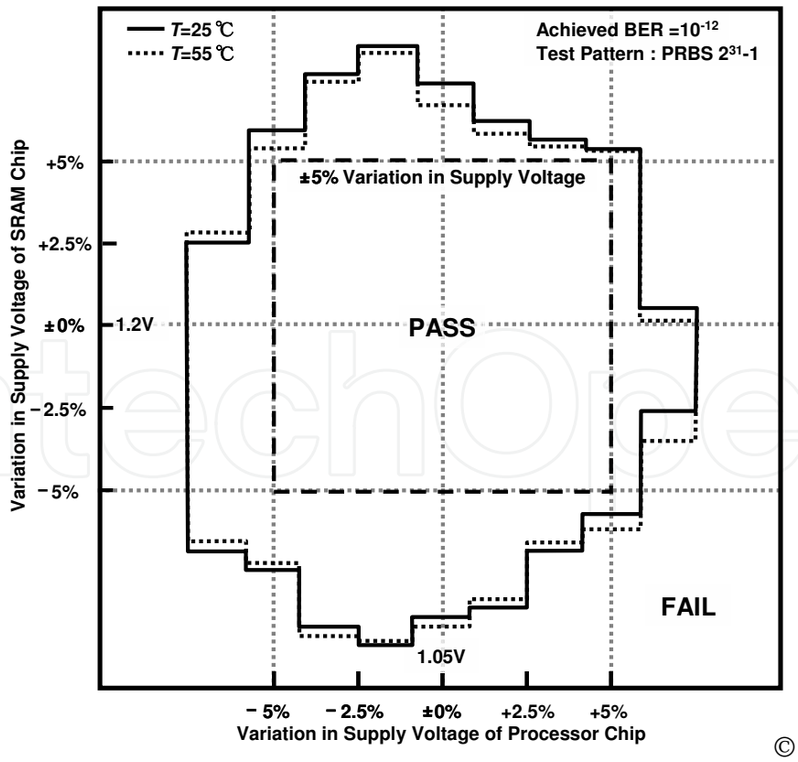

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Fig. 30. Measured tolerance (BER<10^{-12}) to variations in supply voltages and temperature.

inductive-coupling link than mesh type. Additional power dissipation to achieve BER of 10^{-8} is only 9% when signal line drives interconnect of 3mm length. In typical ranges, SRAM array operation does not depend on existence of the inductive-coupling link.
Second, modeling of misalignment tolerance in inductive-coupling inter-chip link is introduced. By comparing the calculated result based on the proposed modeling with the measured result, the modeling was found to be accurate in common cases. The estimated and measured results show that misalignment tolerance of inductive-coupling inter-chip link is high enough to keep the performance under the existence of misalignment in usual condition.
Third, application of an inductive-coupling link to interconnection of commercial MPU and SRAM was performed. By exploiting proposed 2-step adaptive timing adjustment, reliable operation under PVT variation has become possible. Achieved performances are power efficiency of 1pJ/bit and area efficiency of $0.15mm^2$/Gbps, which are 1/30 and 1/3 of conventional DDR2 interface, respectively.

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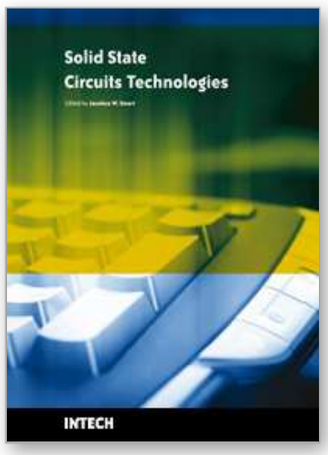

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The evolution of solid-state circuit technology has a long history within a relatively short period of time. This technology has lead to the modern information society that connects us and tools, a large market, and many types of products and applications. The solid-state circuit technology continuously evolves via breakthroughs and improvements every year. This book is devoted to review and present novel approaches for some of the main issues involved in this exciting and vigorous technology. The book is composed of 22 chapters, written by authors coming from 30 different institutions located in 12 different countries throughout the Americas, Asia and Europe. Thus, reflecting the wide international contribution to the book. The broad range of subjects presented in the book offers a general overview of the main issues in modern solid-state circuit technology. Furthermore, the book offers an in depth analysis on specific subjects for specialists. We believe the book is of great scientific and educational value for many readers. I am profoundly indebted to the support provided by all of those involved in the work. First and foremost I would like to acknowledge and thank the authors who worked hard and generously agreed to share their results and knowledge. Second I would like to express my gratitude to the Intech team that invited me to edit the book and give me their full support and a fruitful experience while working together to combine this book.

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