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Metal Gate Electrode and High-$\kappa$ Dielectrics for Sub-32nm Bulk CMOS Technology: Integrating Lanthanum Oxide Capping Layer for Low Threshold-Voltage Devices Application

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1. Introduction

Metal gate electrode together with high dielectric constant or high-$\kappa$ insulator is considered as one of the critical technology enablers to scale the CMOS devices into sub-45nm region (ITRS, 2007; Mistry et al., 2007), due to the following concerns on the conventional poly-Si electrode and Si oxynitride dielectrics stack:

1. Poly-depletion effect to add an equivalent oxide thickness or EOT up to ~0.5 nm to the gate stack, which is a significant portion for the overall targeted EOT requirement of ~1 nm;
2. Excess gate leakage when the EOT of the gate stack is reduced to sub-1nm;
3. High resistance for the poly electrode.

Additional benefit of using metal gate / high-$\kappa$ dielectrics is on the improvement of the device variability as no poly-Si doping is needed. Integration of metal gate /high-$\kappa$ dielectrics using a conventional gate-first route (i.e. the gate stack undergoes a source/drain activation annealing) is attractive as compared to a gate-last route, as the gate first approach is more compatible with the conventional poly-Si/SiON flow, and hence low-cost fabrication is feasible. In addition, in the gate-first flow, the gate stack can afford a high thermal budget process, which is required for embedded application (e.g. DRAM). In this chapter, Lanthanum Oxide, ($\text{LaO}_x$ with $\kappa$ ~20 and an $E_g$ ~ 5.5eV) dielectric capping incorporation into the Hf-based host high-$\kappa$ dielectrics is firstly demonstrated as a practical solution to achieve low threshold-voltage or $V_T$ metal-gated uni-channel nMOSFETs fabricated using a gate-first flow (Kubicek et al., 2007; Narayanan et al., 2006). Further, a comprehensive study is presented on the integration of $\text{LaO}_x$ capping layer for sub-32nm metal gated CMOS devices with Hf-based high-K dielectrics in a gate first manner. Two different integration routes, i.e. Dual Metal Dual Dielectric flow or DMDD (hard-masks to pattern selectively nMOS and pMOS) and Single Metal Dual Dielectric flow or SMDD (soft-mask processes), are presented and compared. The device reliability study is also provided.
2. Experimental

Hf-based high-κ dielectrics, e.g. 1.8nm HfSiO_x with 60% of Hf by metal-oxide chemical vapor deposition, or 1.5nm HfO_2 by atomic layer deposition, were used as host dielectrics. An interfacial layer of ~1nm thermal SiO_2 was formed before high-κ dielectrics deposition. LaO_x capping layer with various thickness was deposited via atomic layer deposition, and incorporated immediately below and above Hf-based high-κ layer. A 10nm Ta_2C electrode by physical vapor deposition or TaCNO electrode by metal-oxide chemical vapor deposition with a 100nm Poly-Si cap layer was then deposited as metal gate. Considering the ultra-shallow junction requirement, source/drain was activated with various thermal budgets: i.e. via Low (1150°C), Medium (1250°C), and High (1350°C) Laser Power anneals (LLP, MLP and HLP), or spike anneals (1035°C). CMOS transistors were fabricated via either DMDD or SMDD approach. Note that Al_2O_3 by atomic layer deposition was used as the dielectrics capping incorporated in Hf-based host dielectrics in pFETs to tune the V_T.

3. Results and discussion

3.1 NFETs V_T dependence on LaO_x capping layer thickness, post-annealing condition, and location

In Fig. 1, it is seen the nFETs V_T (L_g = 1µm) is effectively reduced up to 600mV when increasing the La_2O_3 cap thicknesses. However there is a penalty of considerable mobility degradation for the case of using 1nm think La_2O_3 cap. Thus 0.5nm thickness is considered as the optimum La_2O_3 cap thickness for the device integration described in the following part of this paper.

Fig. 1. Relation between nMOS peak mobility and V_T for different La_2O_3 cap thicknesses on HfSiON with Ta_2C metal gate electrode.
Fig. 2. Ta$_2$C metal gated NFETs $V_T$ dependence on various thermal budgets applied for source/drain activation when positioning LaO$_x$ capping layer above or immediate below HfSiO host dielectrics.

In Fig. 2, the impact of laser annealing conditions (low, medium and high laser power) on $V_T$ of nFETs with LaO$_x$ capping layer positioning above or immediately below HfSiO is shown and compared to the spike- rapid thermal annealed reference. When LaO$_x$ is on top of HfSiO, it is seen that only when applying high laser power, $V_T$ lowering is comparable to the reference sample. On the other hand, device $V_T$ can be effectively reduced regardless the thermal budget applied when positioning LaO$_x$ immediately below HfSiO. It is naturally concluded that the La at the interface between HfSiO and SiO$_x$ interfacial layer plays a critical role to modulate the nFETs $V_T$: In case of LaO$_x$ is on top of HfSiO, when applying high thermal budget (i.e. the high power laser annealing or the spike annealing in this work), La can be driven to diffuse to reach the interface between HfSiO and interfacial layer, effectively driving down the $V_T$. It is worth mentioning that the gate leakage vs. EOT would not be degraded with the adding of LaO$_x$ capping layer into the HfSiO host dielectrics, as shown in Fig. 3, partially due to the excellent $\kappa$ and $E_g$ value of La$_2$O$_3$. Further from Fig. 3, it is noted that Ta$_2$C gated devices exhibit better EOT scalability than the TaCNO case, and the reason shall be discussed in part 3.3 of the paper.
3.2 Integration LaOₓ capping layer into CMOS devices

CMOS transistors were fabricated using both DMDD and SMDD approaches. Fig. 4 outlines the schematic DMDD integration flow. The first gate stack (Ta₂C/ LaO cap/ HfSiO) is deposited (Fig. 4a) and selectively removed from the complementary side using a Si hard mask (Fig. 4b). The second gate (TaCNO/ AlO cap/ HfSiO) is formed again using a Si hard mask (Fig. 4c). Next, the poly-Si is deposited (Fig. 4d) and gate patterning is done by immersion lithography and dry etch (Fig. 4e). The remainder of the flow follows conventional CMOS processing. Cross-sectional high resolution transmission electron microscopy of n- & p- MOSFETs fabricated using DMDD approach with gate lengths of 45nm are shown in Fig. 5 along with a detailed view of the gate stack interfaces after gate etch. The n- & p- MOSFETs boundaries on an inverter circuit can be seen as inset of Fig. 6 (after silicidation). Symmetric low Vᵣ values of ±0.25V can be obtained for both n- and p- MOSFETs (Fig. 6).

In Fig. 7(a), both short-channel n- and p- FETs (Lₐ = 55nm) fabricated using DMDD approach exhibit well-behaved Iₐ-Vₛ characteristics. As shown in Fig. 7(b), the unstrained Iₑₒₑₑ of 1035/500 µA/µm for n- / p- MOSFETs at Iₑₑₑ=100nA/µm and an operating voltage or |Vᵦᵦ|=1.1V are demonstrated on a single wafer.
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Fig. 4. Dual Metal Dual Dielectrics (DMDD) CMOS integration scheme

Fig. 5. XTEM of the n- & pFETs fabricated using DMDD.

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Fig. 6. $V_T$ roll-off for both n- & p- FETs fabricated using DMDD. Inset: SEM views of the nMOS and pMOS boundaries.

Fig. 7. (a): $I_d$-$V_g$ of both n- & p- MOSFETs with a $L_g$ ~55nm; (b) $I_{ON}$-$I_{OFF}$ curves of both n- & pMOS fabricated using DMDD.

Next, we explain the SMDD process flow. As schematically shown in Fig.8, SMDD involves a simple resist-based selective high-$\kappa$ dielectric capping removal process (in this work: La$_2$O$_3$ or Al$_2$O$_3$ over both HfSiO and SiO$_2$). Several key process modules development in this SMDD route is discussed in this section. 1) For the sake of a simple patterning strategy, a wet developable Bottom-Anti-Reflection-Coating or BARC layer is developed to be patterned directly on the dielectric capping and to be selectively removed from the complementary areas (La$_2$O$_3$ from pMOS and Al$_2$O$_3$ from nMOS). This wet BARC layer
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Fig. 8. Single Metal Dual Dielectrics or SMDD CMOS integration scheme

Fig. 9. N-P MOSFETs boundary after etching and resist removal using the wet bottom-anti-reflection-coating or BARC based process (developed for SMDD).

could guarantee an excellent adhesion towards the dielectrics layer, which can not be achieved via 248nm photo-resist only. Fig.9 illustrates the superior adhesion and sharp patterning achieved with wet BARC. 2) The high-κ wet capping removal required for the proposed process flow must be resist-compatible, highly selective (>100) to the underlying layer (SiO₂ or HfSiON). As summarized in Table 1, diluted HCl is the chemistry of choice for La₂O₃, and TMAH for Al₂O₃. 3) Once the high-κ capping has been selectively removed, the
photo resist must be stripped without damaging the exposed materials. The resist strip (NMP- based) and post-cleans (APM- based) process details are provided in Table 1. It’s worthy noting that during SMDD process, both selective high-κ removal and resist strip processes have been characterized physically and electrically indicating no major impact on $V_T$, EOT, gate leakage, mobility and gate dielectric integrity.

<table>
<thead>
<tr>
<th>Resist</th>
<th>Cap removal</th>
<th>Resist strip</th>
<th>Post-clean</th>
</tr>
</thead>
<tbody>
<tr>
<td>La$_2$O$_3$</td>
<td>Wet BARC+ 248 nm</td>
<td>Dilute HCl</td>
<td>Wet organic strip (NMP/AAE)</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>248 nm</td>
<td>During litho development step (1 min ~3.5 % TMAH) (ER 2.4 nm/min)</td>
<td>Wet organic strip (NMP/AAE)</td>
</tr>
</tbody>
</table>

Table 1. Processes used to selectively remove the cap layers (La$_2$O$_3$ or Al$_2$O$_3$) to high-k dielectrics and subsequent strips.

In Table-2, a comparison is made between SMDD and DMDD. The key advantage of SMDD is that the number of process step can be significantly reduced by 40%, which means much lower manufacturing cost. It also allows relatively easier and simpler gate etch profile control since the same metal is used for both n- and p-MOS areas. On the other hand, the $V_T$ tuning flexibility is scarified for SMDD process, as only dielectrics capping layer can be utilized for such a purpose. In contrast, in DMDD process, the combination of dielectrics capping layer and metal gate itself allows a wider $V_T$ tuning capability. In addition, for SMDD approach, attention needs to be paid to avoid the potential impact of capping layer removal process to the gate dielectrics integrity.

<table>
<thead>
<tr>
<th></th>
<th>DMDD</th>
<th>SMDD</th>
</tr>
</thead>
<tbody>
<tr>
<td># of extra process steps compared to conventional SiO$_2$/Si case</td>
<td>15</td>
<td>9</td>
</tr>
<tr>
<td># of extra mask steps</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Gate etch aspects</td>
<td>Different metals etched at the same time</td>
<td>Only one metal etched</td>
</tr>
<tr>
<td>$V_T$ tuning flexibility</td>
<td>cap layer and metal</td>
<td>Cap layer only</td>
</tr>
<tr>
<td>Gate dielectric integrity</td>
<td>Gate dielectric not toughed by removal processes</td>
<td>Gate dielectric only exposed to wet chemistries</td>
</tr>
</tbody>
</table>

Table 2. A comparison between DMDD and SMDD.
3.3 Positive Bias Temperature Instability (PBTI) study of n- MOSFETs with LaOₓ capping layer
The PBTI of nFETs using LaOₓ capping layer is measured at 110°C by using sense-and-measure technique. V_T relaxation with a 100s recovery time after each stress cycle is also measured for dielectric trapping/de-trapping investigation. The measurement set-up is depicted in Fig. 10.

![Fig. 10. PBTI measurement set-up: sense-and-measure method and the V_T relax with 100s recovery time after each stress cycle](image)

![Fig. 11. Stress-field dependent polarity-change PBTI V_T shift is observed in the Ta₂C gated n-MOSFETs when incorporating LaOₓ capping layer, regardless the position (i.e. either on top or immediately below HfSiO). Both laser and spike annealing were applied to the device under study.](image)
Fig. 11 plots the PBTI induced $V_T$ shifts vs. stress times for the Ta$_2$C gated n- MOSFETs. A stress-field dependent two polarities $V_T$ shift is observed, regardless the LaO$_x$ capping layer position (i.e. either on top or immediately below HfSiO). This phenomenon was also reported in the Dysprosium silicate gate stack (Yu et al., 2008), and can be explained by the competition between electron de-trapping (dominate at low-stress field) and electron trapping /defect generation (dominate at high-stress field).

The $V_T$ relaxation on these devices with various source/drain activation processes (i.e. spike or laser annealing) during PBTI recovery periods (100s) is also examined, as shown in Fig. 12. It is observed that the LLP annealed device exhibits a different relaxation behavior as compared to MLP/HLP case, when positioning LaO$_x$- cap either on top or below HfSiO: $V_T$ follows HfSiO-like (i.e. no La) recovery behavior initially and then changes to the La silicate-like gradually as the stress time increases. It is believed that the relaxation behaviors can be explained by the electron de-trap from bulk traps, which are generated by LaO/HfSiO (or SiO) intermixing during PBTI stress, and trap back during the recovery period. Insufficient intermixing is expected for the devices under low power anneal, which not only reduces $V_T$ relaxation amplitude (less trap generation) but also makes relaxation of both Hf-host dielectrics and La-silicate seen simultaneously.

![Fig. 12. $V_T$ relaxation vs. time during PBTI stress for the Ta$_2$C gated n- MOSFETs when incorporating LaO$_x$ capping layer either on top or immediately below HfSiO. $V_{C-V_{Stress}} = 1.25V$ in this case.](image)
In the case of TaCNO gated n-MOSFETs (Fig.13), normal PBTI and pure HfSiO-like $V_T$ relaxation (see Fig.12) are observed. Further, cross-sectional TEM images together with electron-energy loss spectroscopy or EELS study (Fig. 14) suggest the LaO/HfSiO intermixing, and also interactions between dielectrics and electrodes (Ta$_2$C or TaCNO). Interestingly, both image contrast and EELS analysis identifies an oxygen-less region (~1nm) at the bottom of TaCNO electrode. Likely there, the oxygen is incorporated from TaCNO into dielectrics during the intermixing process, and this also links to the worse EOT scalability of TaCNO than Ta$_2$C (see Fig.3 also). Considering these, we thus believe the trapping/de-trapping defects generated from dielectric intermixing are probably related to the oxygen vacancies incorporation (Shen et al., 2004): TaCNO can provide oxygen, suppressing bulk trapping generation in La/Dy based silicates. It is more evident when placing cap layers above high $\kappa$ layer. Schematic diagrams illustrating these phenomena are provided in Fig. 15.

Fig. 13. Normal PBTI $V_T$ vs. stress and $V_T$ relaxation curves vs. time for TaCNO gated n-FETs. Positive $V_T$ and HfSiO-like relaxation behaviors (Fig. 12) are observed.
Fig. 14. (a) Cross sectional TEM shows LaO / HfSiO intermixing after annealing, with both Ta$_2$C and TaCNO electrodes. A less-oxygen layer (or Ta rich) at the bottom of TaCNO electrode is observed from (b) image contrast, and (c) electron-energy loss spectroscopy.
Fig. 15. Schematic diagrams (after thermal anneals) illustrate the negatively charged traps (●) and electron de-trapping (○) during the PBTI stress. Oxygen incorporation from TaCNO can result in less trap generation in the gate stack.

4. Conclusion

A comprehensive study is presented on the integration of LaO, capping layer for sub-45nm metal gated CMOS devices with Hf-based high-k dielectrics in a gate first manner. Two different integration routes, i.e. DMDD and SMDD flow, are reported and compared. The device PBTI study is also provided.

5. References


Mistry K; Allen C; Auth C; Beattie B; Bergstrom D; Bost M; Brazier M; Buehler M; Cappellani A; Chau R; Choi C; Ding G; Fischer K; Ghani T; Grover R; Han W; Hanken D; Hattendorf M; He J; Hicks J; Huessner R; Ingerly D; Jain P; James R; Jong L; Joshi S; Kenyon C; Kuhn K; Lee K; Liu H; Maiz J; McIntyre B; Moon B; Neirynck J; Pae S; Parker S; Parsons D; Prasad S; Ptces L; Prince M; Ranade P; Reynolds T; Sandford J; Shifren L; Sebastian J; Seiple J; Simon D; Sivakumar S; Smith P; Thomas, T; Roeger T; Vandervoorn P; Williams S. & K. Zawadzki. (2007). A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging,
Kubicek S; Schram T; Paraschiv V; Vos R; Demand M; Adelmann C; Witters T; Nyns L; Ragnarsson L.-Å.; Yu H.Y; Veloso A; Singanamalla R; Kauerauf T; Rohr E; Brus S; Vrancken C; Chang V; Mitsuhashi R; Akheyar A; Cho H; Hooker J; O’Sullivan B; Chiarella T; Kerner C; Delabie A, Van Elshocht S; De Meyer K; De Gendt S; Absil P; Hoffmann T. & Biesemans S. (2007). Low $V_T$ CMOS using doped Hf-based oxides, TaC-based Metals and Laser-only Anneal, *Proceedings of Internation Electron Device Meeting*, pp. 49-52, Washington D.C. USA, December 2007, IEEE EDS

Narayanan V; Paruchuri V; Bojarczuk N; Linder B; Doris B; Kim Y; Zafar S; Stathis J; Brown S; Arnold J; Copel M; Steen M; Cartier E; Callegari A; Jamison P; Locquet J; Lacey D; Wang Y; Batson P; Ronsheim P; Jammy R; Chudzik M; Jeong M; Guha S; Shahidi G. & Chen T.C. (2006). Band-Edge High-Performance High-$\kappa$ /Metal Gate n-MOSFETs using Cap Layers Containing Group IIA and IIIB Elements with Gate-First Processing for 45 nm and Beyond, *Digest of Technical Papers, 2006 Symposium on VLSI Technology*, pp. 22.2-1 - 22.2-2, Hawaii, USA, June 2006, IEEE EDS


The evolution of solid-state circuit technology has a long history within a relatively short period of time. This technology has lead to the modern information society that connects us and tools, a large market, and many types of products and applications. The solid-state circuit technology continuously evolves via breakthroughs and improvements every year. This book is devoted to review and present novel approaches for some of the main issues involved in this exciting and vigorous technology. The book is composed of 22 chapters, written by authors coming from 30 different institutions located in 12 different countries throughout the Americas, Asia and Europe. Thus, reflecting the wide international contribution to the book. The broad range of subjects presented in the book offers a general overview of the main issues in modern solid-state circuit technology. Furthermore, the book offers an in depth analysis on specific subjects for specialists. We believe the book is of great scientific and educational value for many readers. I am profoundly indebted to the support provided by all of those involved in the work. First and foremost I would like to acknowledge and thank the authors who worked hard and generously agreed to share their results and knowledge. Second I would like to express my gratitude to the Intech team that invited me to edit the book and give me their full support and a fruitful experience while working together to combine this book.

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