Chapter 1

Silicon Carbide in Microsystem Technology — Thin Film Versus Bulk Material

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Additional information is available at the end of the chapter

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Abstract

This chapter looks at the role of silicon carbide (SiC) in microsystem technology. It starts with an introduction into the wide bandgap (WBG) materials and the properties that make them potential candidates to enable the development of harsh environment microsystems. The future commercial success of WBG microsystems depends mainly on the availability of high-quality materials, well-established microfabrication processes, and economic viability. In such aspects SiC platform, in relation to other WBG materials, provides a clear and competitive advantage. The reasons for this will be detailed. Furthermore, the current status of the SiC thin film and bulk material technologies will also be discussed. Both SiC material forms have played important roles in different microsystem types.

Keywords: silicon carbide, thin film, bulk material, microsystem technology, harsh environment

1. Introduction

As the most popular microelectronic material, silicon (Si) has established itself as the main material for microsystem technology (MST) or micro-electro-mechanical systems (MEMS). This occurred for a number of reasons, including the mechanical properties of silicon (in single crystal form, it is almost a perfect Hookean material and hence no energy dissipation occurs) and economic issues (ready availability of low-cost high-quality materials) [1].

Advances in microsystem technology have frequently been linked to innovations in the development of advanced materials that can outperform conventional semiconductors: not only Si, but also germanium (Ge) and gallium arsenide (GaAs) [2, 3].

In order to enable wide applications in harsh environments, the goal is to develop microsystems able to go beyond the limits of those of conventional semiconductors. In the search for advanced materials to be used in MEMS devices, the wide bandgap (WBG) semiconductors are recognized as the most promising. These semiconductors possess remarkable electronic properties that Si and other conventional materials lack. WBG semiconductors have a high bandgap, more than 2.0 eV, whereas the conventional semiconductors have a small bandgap (around 1.0 eV). One impact of this is that the WBG semiconductor devices can be employed at elevated temperatures [4].

Besides the excellent electronic properties, WBG semiconductors exhibit superior physical properties, as well as chemical inertness, overcoming the limitations of traditional silicon-based platforms in harsh conditions. Thus, WBG MEMS sensing element can be directly exposed to harsh environment media, which may reduce the cost of packaging [5].

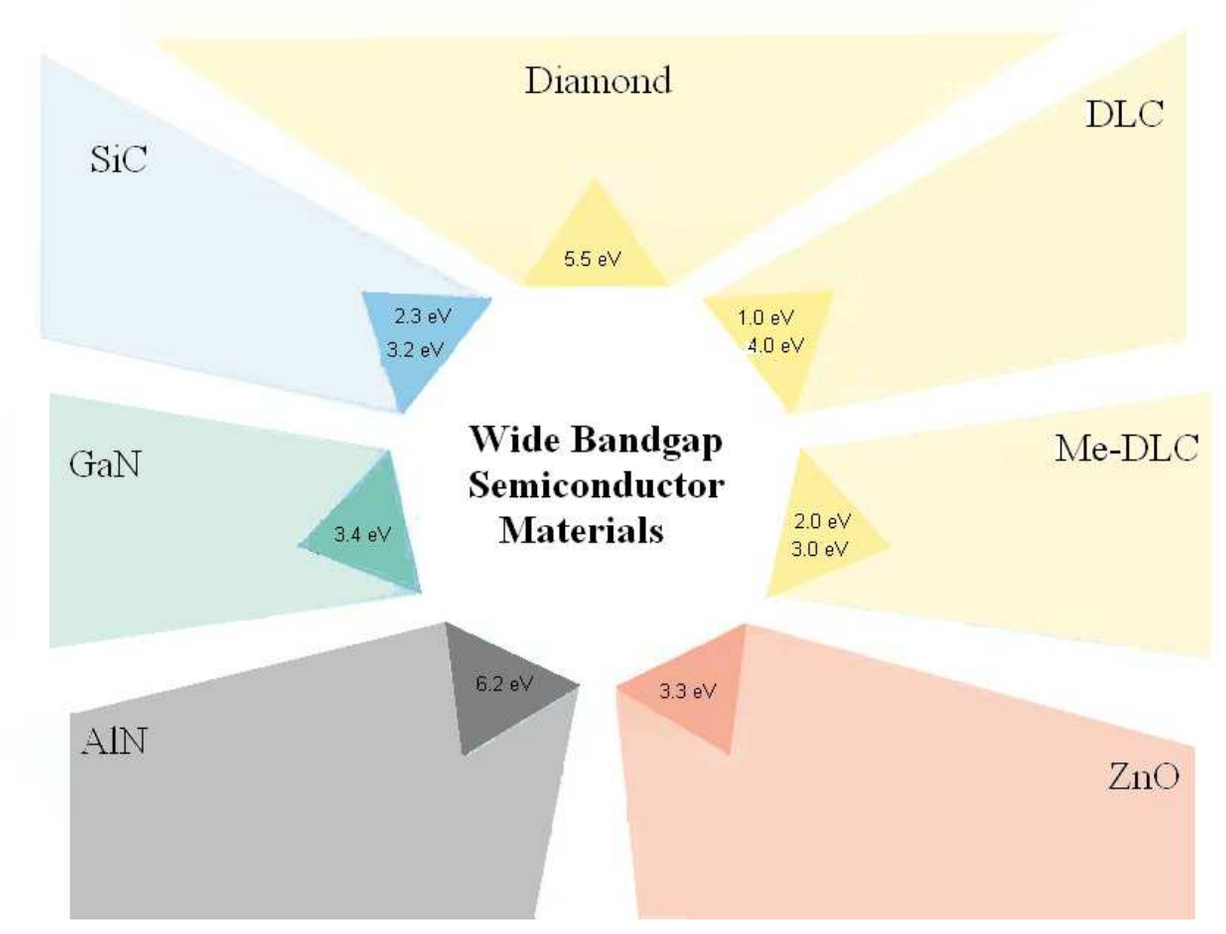

Figure 1. Wide bandgap semiconductor materials with potential for use in microsystem technology

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Other important properties of WBG semiconductors are high Young's modulus, hardness, and fracture toughness. Such characteristics are also potentially interesting for microsystem applications given that the Si has relatively low values [6].

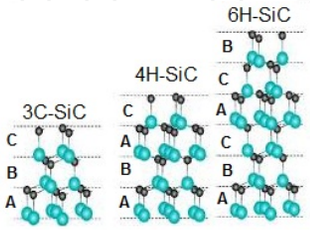
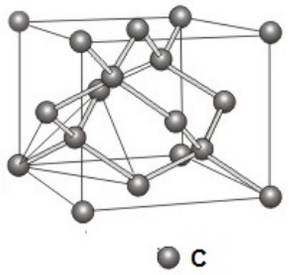
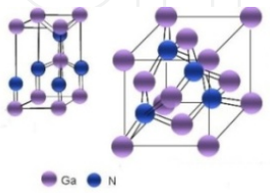
Properties	SiC	Diamond	GaN
Structural	Main crystal symmetries: cubic (zinc blende) and hexagonal (wurtzite) 	Crystal structure: cubic 	Crystal structure: hexagonal (wurtzite) and cubic (zinc blende) 
Physical	• Melting point (~ 2800ºC) • Thermal expansion coefficient at room temperature (4 x 10^{-6} K^{-1}) • Thermal conductivity at room temperature (~500 W m^{-1} K^{-1}) • Dielectric constant (9.7)	• Melting point (~4000ºC) • Thermal expansion coefficient at room temperature (1 x 10^{-6} K^{-1}) • Thermal conductivity at room temperature (2000 W m^{-1} K^{-1}) • Dielectric constant (5.7)	• Melting point (~2770ºC) • Thermal conductivity at room temperature (~170 W m^{-1} K^{-1}) • Dielectric constant (9.0)
Electronic	• Bandgap (2.3–3.2eV) • Electrical resistivity (150 Ω.cm for 3C-SiC, 10^{4}–10^{8} Ω.cm for 6H-SiC and >10^{12} Ω.cm for 4H-SiC) • Saturated electron velocity • (2 x 10^{7} cm/s) • Electric breakdown field (1.2–3MV/cm)	• Bandgap (5.45 eV, indirect gap) • Electrical resistivity (10^{13}–10^{16} Ω.cm) • Saturated electron velocity (2.7 x 10^{7} cm/s) • Electric breakdown field • (10 MV/cm)	• Bandgap (3.4 eV, direct gap) • Electrical resistivity (>10^{5} Ω.cm) • Saturated electron velocity (1.5 x10^{7} cm/s) • Electric breakdown field • (3.5 MV/cm)
Mechanical	• Hardness (~ 30 GPa) • Young's modulus (~ 450 GPa)	• Hardness (~90GPa) and wear resistance • Young's modulus (~1050 GPa) • Strength/tensile (> 1.2 GPa) • Low compressibility • (8.3 x 10^{-3} m^{2} N^{-1})	• Hardness (~10GPa) • Young's modulus (~ 220 GPa)
Optical	• Refractive index (~2.65) • Suited for structural components and mirrors for space-based or ground optical systems	• Refractive index (~2.41) • Optical transparency (UV to far IR) • Highly resistant to damage from irradiation	• Refractive index (~2.3) • Transparency at visible wavelengths coupled with advanced optoelectronic of the nitrides
Chemical	• High resistance to corrosion • Chemical inertness • Biocompatible	• High resistance to corrosion • Chemically and biologically inert	• Radiation-hardened and biocompatible material

Table 1. Properties of SiC, diamond, and GaN

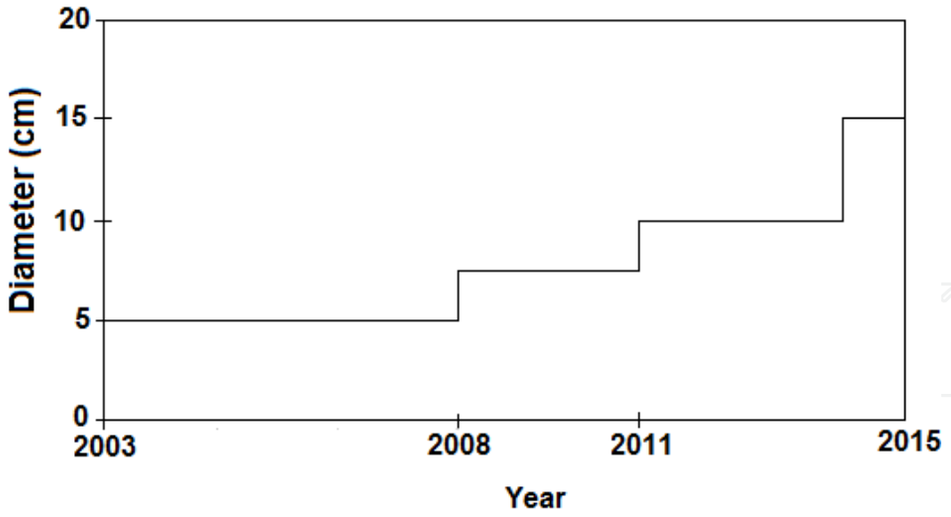


Figure 2. Recent evolution of the diameter of commercially available SiC wafer

WBG semiconductors can be grouped into three main categories: (i) carbon-based materials, (ii) nitride-based materials, and (iii) oxide-based materials. Among them, Figure 1 highlights some examples of WBG semiconductors that are being successful employed in MEMS sensors: diamond [6], diamond like-carbon (DLC) [7], metal-containing DLC (Me-DLC) [8], silicon carbide (SiC) [3], gallium nitride (GaN) [2], aluminum nitride (AlN) [9], and zinc oxide (ZnO) [10].

There is a consensus that the WBG semiconductors are the materials for harsh environment microdevices. However, there are differences and particularities among the different WBG semiconductor types. This leads us to ask which would be the best WBG semiconductors for use in microsystems. SiC, GaN, and diamond are considered with greatest potential due to their outstanding properties (see Table 1) and commercial availability of wafers [11-13]. From a material properties perspective, diamond has superior properties to SiC and GaN, except for its easy oxidation at high temperatures [5].

The technological development of SiC, diamond, and GaN material-based platforms are maturing in three directions: (i) production of wafers, (ii) techniques for micromachining, and (iii) materials integration. These platforms compete with each other. Currently, among them, SiC platform is the most established for harsh environment device applications.

Much progress in terms of quality and dimensions has been made in SiC wafer production. The 4" SiC wafers are the mainstream product on the market and recently 6" wafers were introduced, although the supply is still limited. Figure 2 shows the evolution SiC wafer size in the last years [14]. This diameter increase is crucial for reducing the cost of microdevices through scale economies and the use of Si device fabrication equipment.

In Figure 3, the price per area of SiC substrate wafer is compared with those of Si, diamond, and GaN. SiC substrate is cheaper than other WBG semiconductors [15]. However, the quality is not as good as Si wafers and the cost is significantly higher.

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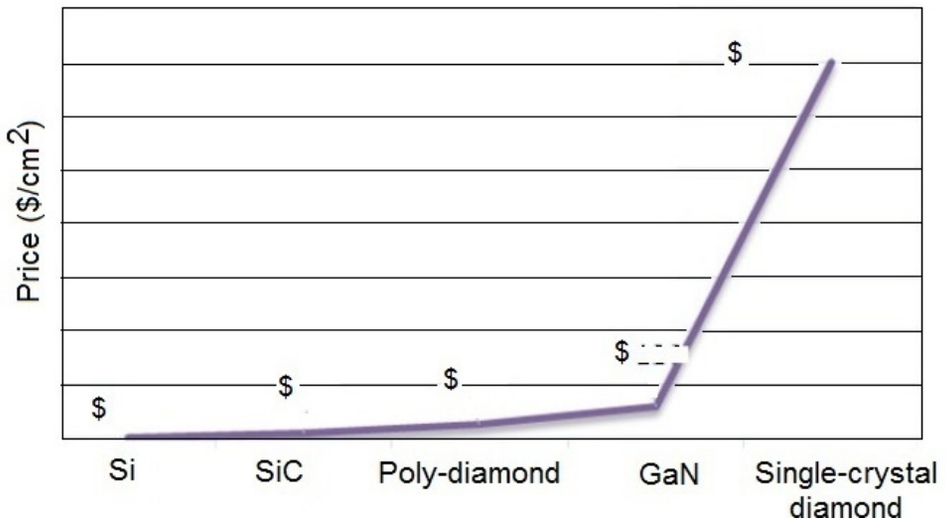

Figure 3. Comparison among the price of wafers of silicon, sapphire, silicon carbide, and gallium nitride (adapted from [15])

Another point related to SiC platform for developing MEMS devices is to establish a fabrication technology comparable to its silicon technology counterpart. One obstacle is the strong chemical stability of high quality SiC bulk, which makes its etching difficult for the fabrication of SiC MEMS structures. To overcome this drawback, the integration of SiC film with Si or SOI (silicon-on-insulator) substrates is a good alternative because it allows the fabrication of SiC-based MEMS through common Si micromachining processes.

Discussion and questions about applications of SiC thin film versus bulk material are opened. There are differences among material properties of each form. However, recent literature has shown that SiC in both forms, thin film and bulk material, play important roles in microsystem technology but each settle into its own role. There are interesting sensing devices that can be produced using both material forms.

SiC thin film has been used in different microsystem devices in different functions such as sensing layer (transduction element), buffer layer, and biocompatible coating. SiC bulk material allows the fabrication of all-SiC microsystem device (structural and sensing elements), which increase its performance especially in harsh environments. According to D. G. Jones's PhD thesis: "One vision of the future is an all-SiC sensor chip composed of crystalline SiC substrate, doped polycrystalline SiC structures, and sputtered amorphous SiC sealing layers" [16].

There is optimism about the feasibility of SiC thin film technology in microsystem applications, but the film growth on large area substrate without loss of uniformity or quality is still a challenge.

The purpose of this chapter is to give an outline of the current landscape of SiC key technologies for microsystem applications. The following SiC technologies are described addressing the bulk material and thin film: synthesis, material properties (quality), material processing, and microsystem device development.

2. SiC material issues for microsystem technology applications

Although there are over 200 known polytypes of SiC, only a few are grown with good reproducibility and attractive properties for microelectronics applications [17]. The polytypes of SiC commonly used in such applications are 3C-SiC, 4H-SiC, and 6H-SiC, which can be synthesized in thin film or wafer forms using different methods. The growth of SiC involves challenges related to the control of (i) polytype formation, (ii) defects, and (iii) doping.

The availability of high-quality SiC material with lower defect density and controlled doping is very important to ensure high fabrication yields and good device performance. For the last couple of decades, the quality of SiC wafer has been significantly improved. Likewise, the growth of high-quality SiC film on Si large wafers is becoming more mature. Unfortunately, thin-film growth methods still seek to obtain 3C-SiC films with properties comparable to those of hexagonal SiC bulk material.

Aside from material growth issues, micromachining of SiC has been the subject of intensive research in recent years for its application in MEMS devices. Several bulk and surface micromachining techniques have been studied for the fabrication of three-dimensional SiC MEMS structures. Nevertheless, despite the advances in deep dry etching methods for SiC bulk micromachining, the process is still complex. On the other hand, SiC-on-Si substrates are attractive for implementing MEMS devices because they combine the well-established Si wet bulk micromachining process with the outstanding sensing properties of SiC thin film.

In the next sections, the issues of growth and micromachining of SiC bulk and thin film will be reviewed.

2.1. Bulk (or substrate)

2.1.1. Bulk crystal growth and material quality

The crystal ingot of conventional semiconductors as Si, Ge, and GaAs are grown by melt methods, which are not suitable for SiC crystal growth because its stoichiometric melting only occurs at pressures above 10 GPa and temperatures higher than 3200 °C [18]. In addition, SiC bulk crystal growth involves challenges attributed to the physical-chemical nature of SiC such as polytypism and extreme thermodynamic properties (noncongruent melting at high temperatures) making difficult the production of semiconductor grade SiC ingots. Figure 4 compares the production of SiC wafers per ingot with ones of Si, sapphire (Al_2O_3), and GaN [19].

Thus as SiC and GaN, sapphire has high melting point and chemical inertness. However, few micromachining processes exist making fabrication of MEMS type structures difficult [20]. So, although sapphire is a promising high temperature material with lower cost, it does not compete with SiC in microsystem applications.

As illustrated in Figure 5, SiC substrates can be grown by methods based on vapor phase or solution phase. The vapor phase growth processes are the most common and are divided in

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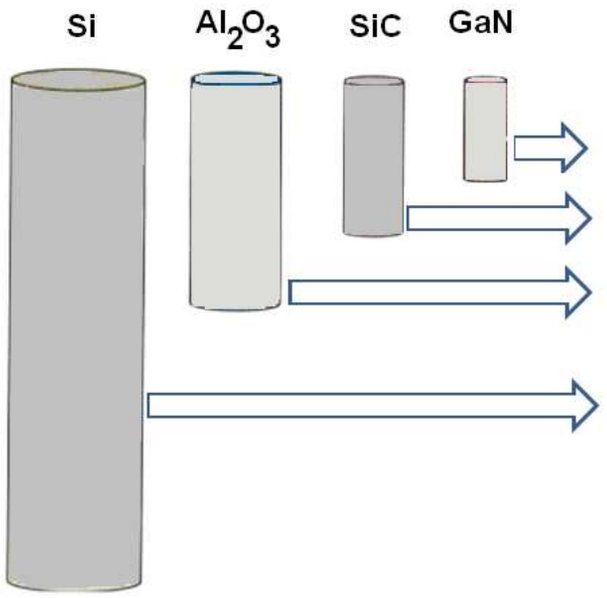

Wafers per ingot	Wafer price
< 10	x 100
< 50	x 30
< 100	x 10
>100	x 1

Figure 4. Comparison among production and price of SiC wafers with ones of Si, Al_2O_3, and GaN

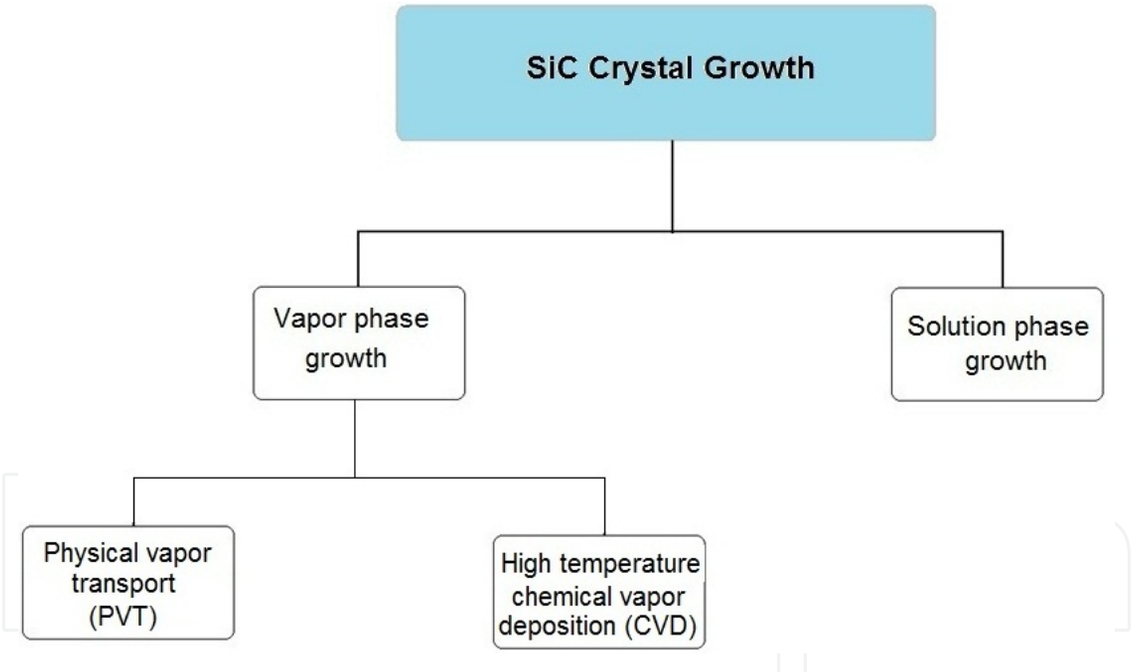

Figure 5. Main methods used for SiC substrate growth

two main types: (i) physical vapor transport (PVT) also called as seeded sublimation method or modified Lely and (ii) high temperature chemical vapor deposition (CVD). With the evolution of these processes, new techniques have emerged, namely, modified PVT method, continuous feed PVT (CF-PVT), and halide CVD [21].

Table 2 summarizes the main vapor phase processes for SiC crystal growth. The first process for growth of high-purity SiC crystal was reported by Lely in 1955. This process allowed the

Method	Description	Drawback	Year
Acheson	The process is based on reduction of silica (SiO_2) and carbon at temperatures above 2000ºC.	In general, the SiC grown by this method is contaminated and not suitable for electronic devices.	1892
Lely	Sublimation of SiC at elevated temperatures (2550–2600ºC) and normal pressure. It was the first method developed for high purity SiC crystal growth.	The control of polytype, size, and doping of the crystal is very limited. SiC crystals only up to 10 mm in diameter.	1955
Modified Lely (seeded sublimation or PVT process)	Polycrystalline SiC at the source sublimes at a high temperature (1800–2600ºC) and low pressure. It is the most mature growth process and allows the production large dimension SiC wafer with good quality.	The control of polytype and doping concentrations is difficult.	1978
HTCVD	SiC growth is carried out using conventional silicon and carbon gas precursors. It is possible to grow long ingots.	Technological challenges harder than for PVT control of the thermodynamic conditions.	1996

Table 2. Description and drawbacks of vapor phase methods for SiC crystal growth

synthesis of SiC with suitable quality for use in electronic devices, which was not possible using the previous method demonstrated by Acheson in 1892. One limitation of the Lely method is the growth of small SiC substrates only up to 10 mm in diameter.

In 1978, Tairov and Tsvetkov modified the Lely method allowing the production of large dimension SiC wafer with good quality. The modified Lely process became the main industrial method for fabrication of SiC wafer substrates of polytypes 4H-SiC and 6H-SiC with different thicknesses and doping (n-type, p-type, and semi-insulating). Regarding the 3C-SiC polytype, the CVD methods have been most used to grow it heteroepitaxially on different substrates, especially silicon. Large monocrystal 3C-SiC substrates with at least 200 micrometers thickness after removing the Si base layer are being produced [22].

Although the thermodynamic properties of SiC do not allow the solution phase bulk growth of SiC from a stoichiometric melt, it is possible to grow SiC from non-stoichiometric solutions containing Si and C. These solution growth processes have been developed based on the solubility of SiC and C in Si melt [21]. A problem is the very low carbon solubility in liquid silicon below 1800°C. It has been shown that the use of Si-metal growth flux is a good alternative to increase the carbon solubility [23]. Despite significant recent progress in solution phase growth, this method is still not well-established to the production of substrates like the PVT and CVD methods.

As pointed out in the previous sections, the wide use of SiC in semiconductor and MEMS devices is limited by high price of high-quality wafers. Controlling different types of defects has been a critical challenge for SiC wafer technology [24].

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In general, defects may compromise the structural integrity of the crystal, or alter its electrical, chemical, and thermal properties. A number of defects in SiC crystals have been reported, including different types of dislocations (mainly open-core screw dislocations called micropipes), low-angle boundaries, macro-inclusions, chemical impurities, and inhomogeneity in either dopant or polytype [25]. Among them, the micropipes are the most common obstacle to the production of high quality SiC devices. The origins of the formation of micropipes during crystal growth are not entirely known, but it seems to involve the propagations of dislocations in the nucleation phase or contaminant particles present upon crystallization [25].

With the continuous improving of wafer manufacturing processes, a significant reduction of micropipe densities has been achieved. Nowadays, there are commercial 2″ and 3″ SiC wafers with micropipe density less than 1/cm^2 and 4″ diameter with less than 10/cm^2 [14]. However, it has been observed that the quality of new larger wafers is relatively lower compared to prior generations [24]. The challenge of SiC wafer technology is increasing the wafer diameter keeping low levels of defects.

2.1.2. Bulk micromachining

Fabrication of MEMS using SiC substrate is still immature when compared to those on silicon substrates or with the SiC power devices. The high thermal and chemical stability of SiC make certain fabrication steps difficult. Etching has required particular attention because etch depths of at least 200 μm are required for bulk micromachined SiC structures [26].

Wet etching in potassium hydroxide (KOH) solution at temperatures between 70ºC and 90ºC is the most used method to fabricate Si MEMS structures due to its advantages like low cost and simple experimental procedure [27]. However, this process is not practical for SiC.

There are no simple wet-chemical etchants for SiC available suitable for device fabrication. Chemical etching is only possible under rather extreme conditions, for example, in molten KOH, NaOH, or Na_2O_2 at 450–600ºC. This process usually creates defects on the surface besides severe contamination from K or Na [28, 29].

The plasma-based dry etching has been shown as a practical way to deep etch SiC for the fabrication of MEMS. Fluorine-based plasmas have the most effective etch rate. An advantage is that the fluorinated etch products (SiF, and CF, species) are relatively volatile, and their removal from the surface is generally not the rate-limiting step [30]. Most commonly plasma sources employed in SiC etching are reactive ion etching (RIE), electron cyclotron resonance (ECR), and inductively coupled plasma (ICP). Much effort has been devoted to understanding the etch mechanisms in these processes in order optimize etching conditions such as pressure, gas flow rate, power, time, etc.

The SiC RIE process has been investigated in fluorinated gases (mainly CF_4, SF_6, and NF_3), usually mixed with oxygen using standard silicon RIE hardware [31]. Generally, SiC RIE process is highly anisotropic with little undercutting of the etch mask, leaving smooth surfaces. Typical RIE etch rate for 4H- and 6H-SiC are in the order of hundreds of angstroms per minute. In this range, the etch rates are sufficient for the fabrication of many electronic devices, but not

for MEMS sensors and some very high voltage power device structures. In such applications, SiC etch rates on the order of tens to hundreds of micrometers deep are required [31].

High density plasma dry etching techniques, such as ECR and ICP, are very promising for deep etching of SiC. The ECR process allows producing very smooth etched surfaces and the control of the degree of anisotropy by the substrate bias. ICP because of high flux with lower-ion energy enables the achievement of excellent anisotropy, low surface damage, smooth morphology, and high etch rate for SiC even at relatively low-bias voltages [32].

A challenge of dry etching processes is the mask. The dry-etch contrast ratio between SiC and typical mask materials as photoresist is low. Thereby deep dry etching requires a hard mask, typically metal such as aluminum (Al), nickel (Ni), or chromium (Cr), to obtain a high etch selectivity [33]. However, many plasma etch systems cannot tolerate the contamination caused by metal etching as a degradation in the health of internal components and electrical shorting occurs [34]. In addition, the presence of a fast-diffusing metal such as Ni within the silicon CMOS fab requires special contamination control precautions [33]. Apart from contamination, during high rate etching, micromasking defects on the etch surface often occurs causing undesirable roughening [34].

Some studies have been conducted to enable the use of non-metallic masks in SiC dry etching, for example, (i) replacing the fluorine-based plasmas by HBr/Cl_2, which allows the use of SiO_2 as etch mask, and (ii) using the AlN as mask material in etching with SF_6/O_2 plasmas [34]. Although both approaches have resulted in etch rate and selectivity lower than those reported to metal masks, a further characterization and optimization of the etch systems can make them promising in SiC MEMS fabrication.

2.2. Thin film

2.2.1. Growth

2.2.1.1. Growth of hexagonal polytypes

The main motivation for the homoepitaxial growth of 4H-SiC is to obtain thick and high quality layers to be used as active regions of power devices and switches with lower losses than conventional silicon-based devices. The 10-kV class SiC P-i-N diodes and insulated gate bipolar transistors (IGBTs) have been fabricated. Furthermore, SiC power Schottky barrier diodes (SBDs), metal-oxide-semiconductor field effect transistors (MOSFETs), and junction field-effect transistors (JFETs) have been already commercialized.

High-quality 4H-SiC epilayers with low defects density are required to fulfill the high performance of SiC power devices. The technology for the realization of bulk 4H-SiC substrates is nowadays well developed but their quality and the possibility to control doping is inferior to the one permitted by epitaxial techniques. Moreover, to realize complex devices, precise control of doping, stacking layers with controlled doping and realization of p-n junction is mandatory. The necessity of very thick epitaxial layers (up to 100 μm) comes from the high bandgap of the material: the breakdown voltage is limited by the depletion region width,

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which depends on the doping level. In order to realize diodes and switches for high-voltage and high power applications, it is necessary to have a material with very low doping concentration, which leads to a very wide depletion layer inside the junction. For this reason, a lot of efforts have been made to develop epitaxial techniques that permit the growth of very thick layers in a reasonable time, maintaining a high material quality.

The 4H-SiC homoepitaxy permits to obtain a material with far superior crystalline quality and lower defect density with respect of 3C-SiC/Si, due to the absence of lattice and thermal mismatch, far superior device performances could be obtained and the adoption of single-crystalline 4H-SiC can significantly extend the range of applicability of MEMS devices in harsh environments. The recent development of photo-electrochemical etching [35] to fabricate MEMS in 4H-SiC increased even more the interest for 4H-SiC homoepitaxy, as will be discussed in the following sections.

The 4H-SiC substrates for SiC homoepitaxy are nowadays commercially available. Due to stacking of Si and C atoms, SiC is a polar material so the substrate surface can actually end with a Si plane or a C plane depending on the crystalline orientation. Si-face substrates are more commonly used because permit to lower the residual nitrogen incorporation with respect of C-face substrates.

Usually, the homoepitaxial 4H-SiC growth is carried out on off-axis substrates, the most common misorientation being about 4° off. It has been found that (0001) vicinal surfaces, due to the presence of surface steps on the growth surface, are able to suppress unwanted polytype formation, thus increasing the crystalline quality. It has also been found that the penetration of basal plane dislocations is effectively hindered in lower off-axis substrates. However, the epilayers grown on these substrates are more prone to form step-bunching and triangular extended defects, due to the presence of terraces [36].

Most of the defects found in the epitaxial layers propagate from the substrate or originate where substrate defects emerge at the surface. It is thus mandatory to deposit SiC onto a substrate with very low defect density, and a lot of effort is thus put in decreasing the substrates defect density, while increasing its size to reduce cost per area.

The most common defects found in the epilayers are: (i) downfalls [37], usually particles formed in the gas phase then precipitated on film surface, (ii) carrots [38, 39], comets [40], or triangular defects [41], elongated defects along the step-flow growth direction, which usually indicate disturbance in the step flow growth. All these defects are known to be device killers and a great effort has been put to optimize the epitaxial growth in order to limit their propagation.

Standard SiC epitaxy is usually carried out in vapor phase epitaxy (VPE) reactors at temperatures between 1500°C and 1700°C, using silane and propane as precursor and hydrogen as carrier gas. The deposition process usually begins with an in situ H_2 etching, in order to improve the substrate surface before the deposition of the epitaxial layer [42]. Depending on reactor configuration and process parameters, etching in H_2+C_3H_8, H_2+SiH_4 or H_2+HCl were also proposed. [43]. Typical C/Si ratios are between 1 and 2, while growth rates for epilayers are usually in the range 5–10 μm/h. However, in order to realize p-i-n junctions and devices

able to block voltages of more than 4 kV, SiC thickness up to 50–100 μm are needed. With such low growth rates the epitaxial deposition needs a very long time and becomes unpractical and expensive. The main problem is that the increase of precursors flow to obtain a faster growth rate results in the formation of silicon droplets in the gas phase, which tends to deplete the nutrient phase and to precipitate on the substrate, thus reducing the epilayer quality. For this reason, the introduction of chlorinated species in the gas phase, such as HCl, methyltrichlorosilane (CH_3SiCl_3, or MTS), trichlorosilane ($SiHCl_3$, TCS), and $SiCl_4$ was investigated. The chlorinated species bind with silicon species in the gas phase because the Cl-Si bond has a lower energy with respect to the Si-Si bond. This permit to avoid the formation and precipitation of Si aggregates and to maintain a mass-transport limited regime where the growth rate is usually linearly dependent on the silane flow. TCS is a precursor of choice of several research groups, since it is safer and more stable that SiH_4 [44]. It brings to the gas mixture both Si and Cl so very high growth rate were achieved using this compound up to 100μm/h without silicon precipitates. Moreover, the use of this precursor has been shown to reduce defects such as basal plane dislocations, point defects, and single Shockley faults. Also, a smoother surface, with root means square roughness as low as 0.18 nm, was demonstrated. Another method to overcome Si reactions in the gas phase is to lower the reactor pressure up to 20–40 mbar but it is not as effective as the chlorine addition.

In order to realize SiC power device, an accurate control and optimization of doped layers is necessary. Doping concentration and uniformity over the substrate area and on all the substrate in a planetary reactor are key-issues for the performance of the devices. The N-type doping is usually carried out with nitrogen.

Nitrogen incorporation has been found to be enhanced by Si-rich gas phase, because N atoms substitute C sites in SiC lattice. P-type doping is less common in literature but is nevertheless very important for devices such as pin diodes and IGBTs. The most common dopant for the growth of p-type layers is aluminum, usually in the form of trimethyl aluminum (TMA). Aluminum tends to substitute Si in the lattice, and it was generally found to depend on the C/Si ratio: at higher values the p-type doping was found to increase. Also, it was found to decrease with the Cl/Si ratio [45].

2.2.1.2. Growth of 3C-SiC films

Cubic silicon carbide (also called 3C or β) shows similar interesting features as the other polytypes, such as wide bandgap (2.39 eV), high breakdown field (2.2×10^6 V/cm), high thermal stability and conductivity, mechanical strength, Mohs hardness of roughly 9, and a Young's modulus that ranges between 330 GPa and 700 GPa depending on the polytype and measurement technique used to acquire the data. In addition to that, 3C-SiC has some peculiar features that fostered the attention of researchers. Among the three most common polytypes (3C, 6H, 4H), the cubic one has the highest saturated drift velocity (2.5×10^7cm/s), which allows to obtain high channel currents in microwave devices [46] and it is helpful for high gain solid state devices. Owing to the higher symmetry and consequently a reduced phonon scattering, 3C-SiC has also the highest electron mobility (≈1000 cm^2/V.s) compared to the other polytypes. The mobility is directly linked to the conductivity of a semiconductor and having a high

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mobility means to be able to obtain a higher current. This will lead to faster capacitance charge. In general, a device built with a high mobility material has a better high frequency response. A high maximum current density is fundamental to increase the number of components per integrated circuit chip, to target large-scale integration. The thermal conductivity of cubic SiC is significant (3.2 W cm^{-1} K^{-1} (poly-3C)) even if compared to those of the most common metals, although slightly lower than other polytypes (3.6 W cm−1 K−1 for 6H–SiC and 3.7 W cm−1 K −1 for 4H–SiC). Additionally, cubic SiC is more and more used as a substrate for the epitaxial deposition of other materials such as gallium nitride [47] or boron nitride [48].

The feature that most determines the success of the applied research on cubic SiC is the possibility of epitaxial growth on silicon, which also has a cubic lattice, but with different constant (≈20% lattice mismatch) [49]. Cubic SiC may also be heteroepitaxially grown on 6H-SiC [50] and on TiC [51]. In addition to that, the bulk SiC contains screw dislocations that can propagate into the epitaxial layer, as in the case of 4H-SiC [52], while it is possible to find nearly defect-free silicon wafers. The availability of silicon wafers with diameter up to 17.7 inches compared to the smaller diameters of commercially available SiC, together with the extreme difficulties to obtain single crystal, large area bulk 3C-SiC crystals, pushed toward silicon the choice for the preferred substrate for 3C-SiC epitaxy. Moreover, the lowering cost of silicon wafers, even for high quality substrates, may help to bring the benefits of SiC technology to consumer devices.

There are many technological advantages using SiC on Si, like the easy integration in silicon electronics, which is already extremely developed and almost ubiquitous. Silicon and silicon carbide have also the same native insulating oxide that might be exploited for the processing and fabrication of Si-SiC-based electronic devices.

The silicon lattice constant is 5.43 Å, while in 3C-SiC it is 4.36 Å, which results in a lattice mismatch of approximately 20% and it can lead to a highly defective epitaxial film, which can be detrimental for electronic devices. The substrate thickness is much higher than the epilayer in the first stages of the growth and this leads the strain to be positioned almost completely in the deposited layer. The effect is the presence of shear stresses in crystal planes that may cause defects formation when a critical thickness of the epilayer is reached. In addition to that, the different thermal expansion (≈8% difference between Si and SiC) fosters the formation of defects during the cooling stage after the growth [53]. A brief review on the defects generated in the SiC layer and strictly correlated to the heteroepitaxy on silicon such as misfit dislocations, twins, stacking faults, threading dislocations, antiphase (or inversion) domain boundaries (APBs on Si (100)), and double positioning boundaries (DPBs on Si (111)) is presented in the next section.

In order to try to reduce the effect of the different lattice parameters between Si and SiC, a carbonization process is often used in the first stages of the epitaxial synthesis. Flowing carbon precursors as propane, methane, or ethane at high temperature over the silicon substrate is a well-known technique [54] to create a thin layer of SiC on the surface of the silicon substrate. Since the SiC lattice parameter is lower than the one of Si, in many cases atoms with bigger size like germanium [55] are added during this process.

Frequently the terms "carbonization" and "buffer layer" are mixed up in literature, but in this work we will refer to carbonization as the process performed only with the carbon precursor turning the outer layers of the silicon substrate into silicon carbide. Other precursors may be added, but not the one for silicon, as it happens in the "buffer layer" process, as reported hereafter. Another technique to ensure the relaxation of elastic energy at the interface between the substrate and the epilayer and to help to stop the propagation of the defects generated at Si-SiC interface is the introduction of a buffer layer prior to the growth. This can be made of silicon and carbon or other materials with less difference in lattice parameters. Typically, the gradual matching between the substrate and final overlayer is ensured via a continuous composition gradient of the buffer layer. A common way to reduce the strain is to pattern the silicon substrate in order to grow SiC crystal with a finite size. The first material used and the most common one to manufacture the mask is silicon oxide [56, 57], but other materials like silicon nitride or aluminum nitride also proved to be effective [58].

The difference in lattice parameter between Si substrate and SiC epilayer causes an "island" growth mode in the very first stages and then may originate many defects in the epitaxial layer, the most common being misfit dislocations, stacking faults and antiphase boundaries.

Misfit dislocations are generated at the interface between the substrate and epilayer, in order to allow the minimization of the lattice strain. The misfit dislocation leaves dangling bonds at the interface and it may propagate as a threading dislocation in the epitaxial layer often causing high leakage currents in a Si/3C-SiC device. TEM images help in understanding the phenomenon (see Figure 6 from [59]): five (111) SiC lattice planes match with four (111) silicon planes, which correspond to a 20% lattice mismatch. In the case of silicon carbide grown over silicon, the difference in the two thermal expansion coefficients contributes to create additional misfit dislocation during the cooling stage after the growth, in order to relieve the stress created at the interface between the two crystals. The voids are another typical defect at the SiC/Si interface that are formed due to outdiffusion of Si during the heating process. If the carbonization is not properly optimized and if a continuous, thick SiC layer is not formed after the low temperature carbonization, during the second heating up to the growth temperature Si outdiffusion from the substrate may occur, leaving voids of the dimension of some μm^2 at the interface [60]. These defects may degrade the electrical properties in vertical devices, where current flows in the Si substrate. Also, the presence of voids may disturb the SiC lattice arrangement above them, thus increasing the concentration of extended defects.

A two-dimensional deviation of the position of the atoms from their corresponding lattice site is called generically "planar defect." The most common types found in heteroepitaxial silicon carbide are stacking faults (SF), twins, and antiphase boundaries (APB).

Stacking faults are an anomaly in the stacking sequence of the different layers (ABCABCABC for 3C, ABABAB for 2H,...) of the crystal. This can be also considered as a local occurrence of another polytype**.** The energy associated with this kind of defects is very low, if compared to other planar defects, because this does not affect the near neighbor bonding; therefore, it is very common to observe stacking faults in cubic silicon carbide along the stacking of {111} planes. It is appropriate to remember that there is almost the same interface spacing between hexagonal and cubic planes [61].

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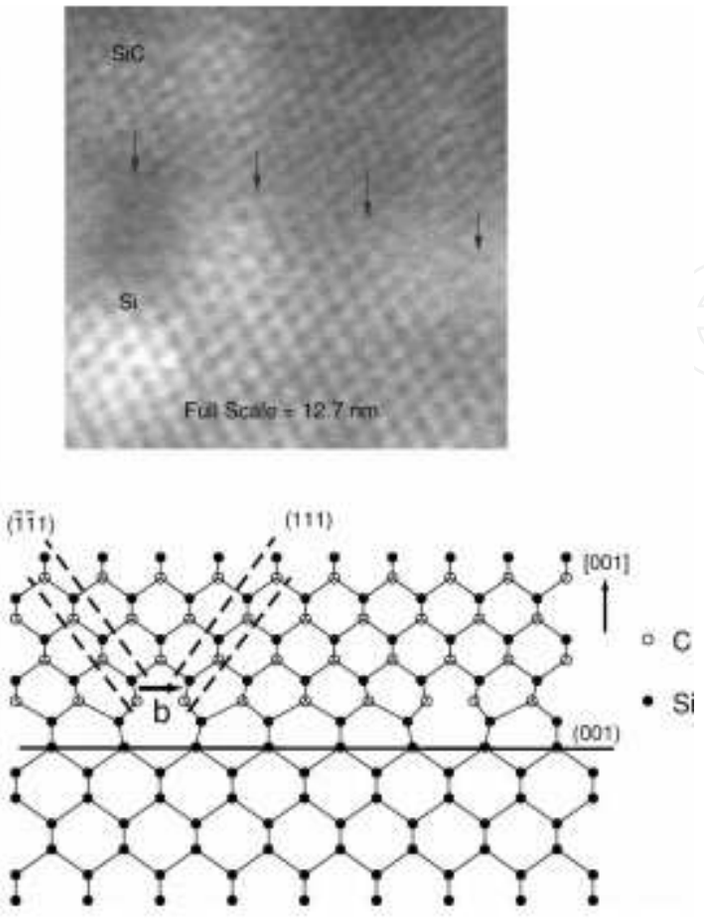

Figure 6. Lattice arrangements at the SiC/Si interface [59]

A twin is a particular defect in the stacking sequence of the planes in which the sequence at the opposite side of the defect plane is mirror images of each other. For example, in the cubic polytype, where the stacking sequence is ABCABCABCABC..., a twin may occur like this: ABCABCBACBACBA. This corresponds to a change in the crystal orientation.

As said previously, the lattice mismatch between the substrate and the epilayer causes the growth of three-dimensional islands in the first stages of the synthesis process known as "island growth mode." The genesis of antiphase boundary domains (APB) is linked to the non-perfect planarity of the substrate. In addition to the initial roughness of the silicon, which to-date can be significantly reduced, the carbonization process introduces many irregularities. During the island growth mode, islands generated in different sites of the substrate may be at different levels owing to the presence of surface steps on the substrate. During the growth and coalescence of the islands, a Si outer layer of an island may bond with a Si layer of another island, thus forming Si-Si bonds. The same phenomenon may occur with C layers of two different islands generating C-C bonds. These boundaries usually propagate along (111) planes, and when two boundaries with opposite orientation combine, they annihilate themselves and the result is the disappearance of the island (and of the APB).

It is possible to generate double position boundaries (DPB) on SiC grown on a (111) surface. This kind of defect is the result of twins that start from the epilayer-substrate interface. The epilayer may orient with respect to the substrate in two ways that are crystallographically equivalent but are rotated 60° relative to each other. When two growth nuclei with different orientations coalesce, a DPB is formed.

2.2.2. Epitaxial SiC quality

Epitaxial 3C-, 4H-, and 6H-SiC have very different properties and characteristics, mainly because of the hetero or homo-epitaxial processes necessary for their deposition. The main issues affecting SiC material quality are due to the substrate used and the growth process. The quality of grown material can be measured mainly in terms of lattice perfection (e.g., from XRD measurements), point defects, extended defects, and residual strain. Usually, the presence of crystalline defects does not hinder the performances of MEMS devices or their capabilities to work in harsh environments.

Due to the ease of fabrication on Si substrate, the polytype of choice for the realization of SiC MEMS is still 3C, and in this case there are still more variables to be considered because this polytype can be deposited in different forms such as crystalline, polycrystalline, or amorphous. These lattice structures have different mechanical properties, such as Young's modulus, which may affect MEMS fabrication.

The mechanical properties of polycrystalline 3C-SiC depend on its characteristics such as preferred orientation, stoichiometry, grain size and shape, and defect. Polycrystalline SiC films have a lower Young's modulus with respect to single crystalline SiC [62], and amorphous films growth at lower temperatures may have even lower Young's modulus values [63]. The Young's modulus of high crystalline quality of 3C-SiC/Si was found to depend on thickness [64] ranging from $1.5x10^{11}$ to $3.75x10^{11}$ Pa for thickness between 2 and 3 μm. Considering that the epitaxial quality of SiC increases with thickness due to progressive annihilation of defects and lowering of (002) XRD peak FWHM, the increase in Young's modulus with thickness could be related to lattice quality and defect density. This is one of the most important characteristics to be considered when designing MEMS and still hinder the development of microfabrication. Different growth processes may lead to completely different microstructure properties due to the presence of different type and density of lattice defects and strain content.

In the case of most common MEMS devices, the main requirements of the material are related to mechanical strength and hardness. The presence of residual stress or stress gradients inside the epitaxial layer can also hinder the process of microfabrication in different ways. The stress, originating either from lattice and thermal mismatch in 3C-SiC/Si heteroepitaxy, may cause severe macroscopic bending of the substrate, and may make photolithographic processing impossible or very difficult. At the microscopic level, stress and stress gradients may bend the microstructures or introduce unwanted and unpredictable forces to the system that may alter the behavior of the device or change the predicted resonant frequencies. Different strategies may be adopted to minimize the strain content of 3C-SiC/Si, from the carbonization process optimization or to the deposition of special buffer layers to reduce the lattice mismatch strain

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[60]. However, the presence of thermal mismatch cannot be avoided and could be limited only by reducing the growth temperature.

Reducing the deposition temperature has a tremendous effect on 3C-SiC. High quality crystalline material, with XRD FWHM peak as low 200 arcsec, is usually grown at temperatures higher than 1250–1300°C, with temperatures in the range 1350–1400°C being most commonly used. Precursors of choice are silane and propane, in hot wall VPE reactors. Lowering the growth temperature usually means to significantly degrade the surface morphology and to increase the roughness. In order to maintain a high material quality even at lower deposition temperatures, several alternative precursors have been studied and plasma enhanced techniques have been used. Most of alternative precursors include a Si-C bond in the molecule, such as tetramethylsilane, methyltrichlorosilane, monomethylsilane, hexamethyldisilane, and have lower cracking temperature. However, since for standard MEMS processes the suitable surface termination or the high crystal quality are not mandatory requirements, a trade-off between process conditions and 3C-SiC characteristic may be found. Different deposition techniques such as chemical vapor deposition (CVD), plasma enhanced CVD or sputtering are normally used to deposit polycrystalline or amorphous 3C-SiC at low temperature. Doping of poly or amorphous remains an issue because grain boundaries inhibit dopant incorporation and carrier transport. Moreover, dopant species must crack at low temperature so normally NH_3 (which is toxic) is normally used instead of N_2.

Doping can also influence important properties like crystal quality and strain. The increased doping concentration results in a slightly decreased or increased lattice constant, because N substitute C in the SiC lattice and Al substitute Si for p-type doping. Doping affects thus not only the electrical properties but also the mechanical properties, such as elastic modulus and hardness, so that it can influence the resonance frequency of microstructures. Elastic modulus and hardness of the 3C-SiC thin film may decrease from 350–400 GPa to 150–200 GPa and from 35 GPa to 20 GPa, respectively, with an increase in the nitrogen concentration [65].

2.2.3. Surface micromachining

As it was discussed previously, SiC MEMS has a tremendous potential for the realization of devices operating in harsh, biological environments and high temperatures, exceeding the capabilities of current silicon technology. The polytype of choice for the realization of SiC MEMS is still 3C, either polycrystalline or heteroepitaxial deposited on Si, SOI, or on a sacrificial layer such as SiO_2 or poly-Si. Its main limitations are still due to the low material quality (low crystallinity, high concentration of lattice defects) and the high amount of residual strain due to the heteroepitaxy. However, advances in 3C-SiC epitaxial techniques and the possibility to use well-developed silicon wet-etch techniques to realize SiC MEMS provided a convenient way to fabricate even complex devices. Suspended 3C-SiC structures are released by surface machining using both the wet and dry etching process.

Microfabrication technology on 4H-SiC is much more complicated than the 3C-SiC/Si system because of the lack of a wet etchant for 4H-SiC: conventional wet chemical etching of SiC is not possible at a practical temperature and with suitable etch rates. 4H or 6H-SiC MEMS were

fabricated by expensive and complex techniques such as wafer bonding or smart-cut technique [66], anisotropic electron cyclotron resonance (ECR) etching technique [67], or bulk micromachining [68] from the backside of the wafer. However, the possibility to combine active electronics and microsystems in a single device that could withstand extreme environments and high power is very promising.

2.2.3.1. Processing techniques

SiC can be processed with many of the techniques used also for silicon, while, owing to its mechanical hardness and chemical inertness, not all of the silicon etching techniques can be used for silicon carbide.

Oxidation

It is possible to grow stable thermal oxide layers on all SiC polytypes, as it is commonly done for silicon, but the oxidation rate is much lower. Owing its chemical stability SiC is less likely than silicon to dissociate and react with oxygen to form silicon oxide. Furthermore, CO, one of the reaction products, must diffuse out of the oxide layer for the reaction to proceed. Even if the presence of hydrogen or water vapor increases the oxidation rate, frequently, a thick oxide is required for MEMS fabrication; for this reason the deposition of polycrystalline silicon and following oxidation [69] or the direct deposition of silicon oxide is generally chosen.

Metallization

The deposition of different metallic species to achieve good ohmic or rectifying contacts on SiC has been widely investigated. Depending on the deposition parameters, but mostly on the annealing temperature, different contact behavior can be obtained ceteris paribus.

Annealed Ni for n-type SiC or Al for p-type have been extensively used to obtain ohmic contacts with low contact resistivity [70, 71], while Au [71], Ti [71], Pt [72], or Al [73] have been studied to obtain Schottky barriers. Nevertheless, using some metal that prevents the exploitation of silicon technology, as gold, the metallization should be performed outside of IC fabrication facilities because gold shows electromigration at relatively low temperatures.

SiC-coated MEMS

One can exploit the well-developed state-of-the art of silicon micromachining techniques to obtain devices with complicated design using well-known silicon etchings and covering them with monocrystalline or polycrystalline silicon carbide after the MEMS is released. It has been shown that depositing a thin SiC film over a silicon MEMS improves significantly the wear resistance, decreases the static friction, thus enhancing the device lifetime [74]. The erosion resistance typical of silicon carbide is exploited for SiC-coated MEMS operating in chemically harsh environments [75]. In prospect, the direction of MEMS development will be toward an additional size reduction. For this reason, another feature that is gathering interest is the reduction of adhesion of SiC-coated MEMS [75] thanks to the reduction of surface forces owing probably to topographical surface properties and slower oxidation rates.

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SiC on insulator substrates

There is a great interest in obtaining SiC-on-insulator (SiCOI) substrates for micromachining both for obtaining electrical insulation of the SiC layer from substrate and to use oxide as a sacrificial layer or etch stop.

Silicon-on-insulator (SOI) substrates are obtained by ion implantation of O into the subsurface region of Si wafers, or, more frequently, bonding two silicon wafers covered by oxide. The first attempts to achieve a 3C-SiC layer over silicon oxide starting from a SOI were reported by Reichert et al. [76]. This method has some challenges: the buried oxide quality must be high to withstand the elevated temperatures needed for growing monocrystalline SiC (typically high T, near silicon melting point, 1414°C, ensure better quality epitaxial SiC, but for MEMS a lower crystalline quality may be acceptable). When silicon oxide reaches high temperatures, it undergoes glass transitions [76] and starts to degrade leaving a holey structure (outdiffusion of oxygen [76]) and worsening the electrical characteristics. Another important challenge is the complete conversion of the silicon overlayer into silicon carbide, if not, an undesirable 3C-SiC-on-Si-on-SiO structure is obtained. The carbonization step, as explained in the epitaxial growth part of this chapter, may help in obtaining that, but the method is limited because the diffusion process can reach a limited thickness (around 200 nm in the Si layer). Finely tuning the growth parameters, the production of SiCOI without significant degradation of the buried layers was demonstrated [77].

The "smart cut" process was already developed for obtaining SOI [78, 79]. The process starts with two oxidized silicon substrates, called handle wafer and implant wafer. Hydrogen ions are implanted into the implant wafer under the oxide layer and buried in the silicon bulk at a low depth. After the bonding of the two wafers, an annealing is performed and the implanted hydrogen forms a void layer inside the silicon. After that it is possible to break the implant wafer along these voids leaving the thin silicon layer still bonded to the handle wafer. The same process was successfully used using 6H-SiC substrates with 1-μm-thick deposited oxide layer as implant wafer and 6H-SiC, polycrystalline SiC, and Si layers as handle wafer [77] thus obtaining SiCOI.

As for SOI, wafer bonding is also used to obtain SiCOI [77]; in this case the handle wafer is thermally oxidized silicon. A film of cubic silicon carbide is epitaxially grown on a silicon wafer, and silicon oxide is deposited on this SiC layer. The two wafer oxide surfaces are treated and bonded together, then the handle wafer is protected and the silicon is removed from the second wafer generally using wet etching techniques. The result is a 3C-SiC-on-insulator-on-silicon structure. In literature it is possible to find other wafer bonding processes to obtain SiCOI, such the polysilicon-polysilicon bonding technique [80].

3. A brief overview of the most common SiC microsystem devices

Silicon carbide exhibits piezoresistive and piezoelectric properties as well as superior thermomechanical properties at higher temperatures (>300° C) [81]. Thus, there is a growing

interest in its use as an electromechanical material to replace the silicon in a variety of potential harsh environment applications. Microsystems have become an important direction for SiC technology development. Currently, SiC is the wide bandgap semiconductor material with most potential for MEMS sensors and actuators.

The resonators are one of the most investigated SiC MEMS. SiC resonant structures can present much higher resonant frequencies compared to the same dimensioned Si or GaAs structures due to its high Young's modulus and the relatively low mass density [82]. SiC MEMS resonators have been fabricated with higher power handling capabilities and operating frequencies, compared to those of similar polysilicon-based resonators [81]. Two types of SiC-based resonators have been reported, which use: (i) SiC grown on Si (or SOI) substrates and (ii) homoepitaxial layer grown on single-crystalline 4H- or 6H-SiC substrates.

SiC resonators can be easily fabricated on Si substrates using surface micromachining fabrication technology. This fabrication process is attractive because of integration compatibility with CMOS processes, low-cost film deposition, and minimal compromises between the electrical and mechanical performances of the fabricated structures [81]. Wang et al. reported the fabrication of MEMS resonators based on SiC thin film deposited by low temperature PECVD [82]. These resonators were tested and showed a good performance for harsh environment, such as, high temperature, erosion, and high pressure. The use of mono- and polycrystalline 3C-SiC grown on Si wafers by CVD in resonators able to work at high frequencies with high quality factors has also been reported. The structure of the 3C-SiC resonator is schematized in Figure 7(a) [83].

Regarding the resonant structures made of homoepitaxial layers grown on single-crystalline 4H- or 6H-SiC substrates, their fabrication process is more difficult than that of SiC/Si MEMS. However, high resonant frequency makes 4H-SiC MEMS very attractive for high-sensitivity sensors. Adachi et al. compared the resonance characteristics of 4H-SiC cantilevers on 4H-SiC substrate with the same dimensions of 3C-SiC cantilevers fabricated on Si substrate. It was observed that the resonant frequency of the 4H-SiC cantilevers was 10 times that of 3C-SiC cantilevers [84]. The 4H-SiC cantilevers were fabricated by doping-type selective electrochemical etching of 4H-SiC and their structure is shown in Figure 7(b).

Recently, Yang et al. reported high frequency torsional resonators based on a single-crystal 6H-SiC thin layer on top of a SiO_2-on-Si wafer by using a "smart-cut" process. 6H-SiC smart technology is an alternative process to micromachining of 6H-SiC, which is not only very time consuming but also requires deposited metal masks and still lacks precision when thin films and small dimensions are required for devices [85].

Another important type of SiC MEMS is the piezoresistive sensors for harsh environment applications. In the 1990s, the first piezoresistive pressure sensors developed on 6H-SiC substrates were reported for applications up to 500ºC [86, 87]. These sensors were batch-microfabricated using a combination of photo and dark etching methods to create the diaphragm. In 2004, Ned et al. reported the fabrication of 6H-SiC pressure sensors, with optimized sensing diaphragms containing "bossed" areas, using a combination of deep reactive ion etching (DRIE) and electrochemical etching [88]. The reports on 4H-SiC pressure sensors are

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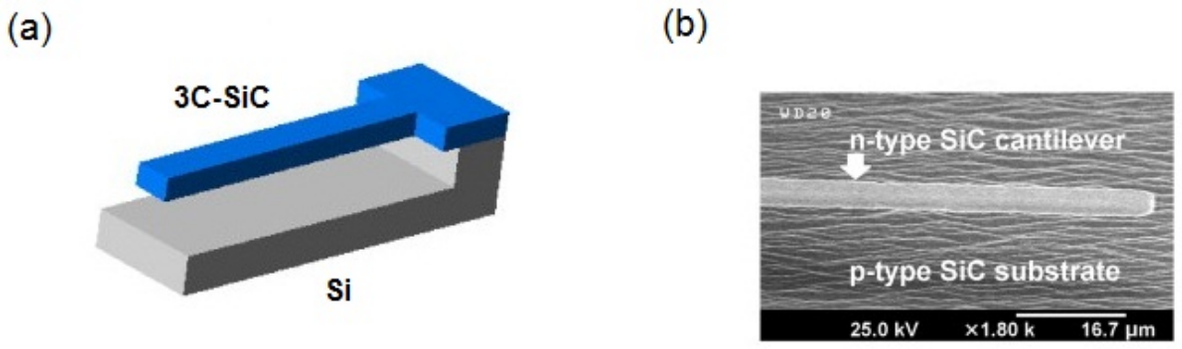

Figure 7. (a) 3C-SiC resonator structure [83] and (b) 4H-SiC micro cantilever [84]

more recent than those of 6H-SiC. In 2011, Akiyama et al. introduced a new approach for the fabrication of 4H-SiC bulk sensors using a mechanical milling (drilling) to form the membrane of the sensor. The detailed milling process done by Tecnisco (Japan) was not disclosed [89]. Earlier this year, Okojie et al. investigated 4H-SiC piezoresistive pressure sensors when operated up to 800ºC. This is the first experimental work published under piezoresistance versus temperature for 4H-SiC [90].

On the other hand, the piezoresistive properties of 3C-SiC and a-SiC films and the influence of the temperature on them have been reported by different authors as reviewed in [91]. The first studies were focused on polycrystalline 3C-SiC films. However, recent publications have demonstrated that a p-type single crystalline 3C-SiC film is a valuable material for MEMS sensors [92, 93].

The potential of SiC for gas sensors in a range of environments has also been reported [94, 95]. These sensors exhibit a simple sensing element based on metal-insulator-semiconductor (MIS) structure, typically a capacitor or a Schottky diode. The use of an insulating layer separating the metal from the SiC allows these devices to operate at temperatures in excess of 900°C [94].

4. Summary

The wide bandgap semiconductor technologies are the key to enable the development of MEMS devices for harsh environment applications. Among them, SiC technology is the most mature from the viewpoint of material quality, manufacturing, and device performance. High quality single crystal wafers are commercially available; wafer size and substrate qualities are increasing whereas wafer cost is decreasing. In the same way, thin film growth techniques have been optimized to accurately synthesize SiC with the necessary properties for its device applications such as material composition, crystal structure, suitable electrical conductivity, morphology, and mechanical characteristics. Despite these advancements in the manufacturing of SiC wafers, thick films, and thin films, there are still processing challenges especially related to doping and micromachining. SiC bulk etching techniques have been developed

seeking high throughput to realize patterned, high-aspect ratio features, such as preservation of sidewall smoothness and etching profile at high etch rates, and high selectivity. In parallel, the progresses on the growth of 3C-SiC on silicon substrates and in surface micromachining techniques have enabled the fabrication of interesting MEMS devices.

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