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Investigation of Sensitivity to Heavy-Ion Irradiation of Junctionless Double-Gate MOSFETs by 3-D Numerical Simulation

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1. Introduction

Microelectronics industry has experienced tremendous progress in the last forty years, especially with regard to the evolution of the products (i.e. integrated circuits) performances, and at the same time, concerning the drastic reduction of manufacturing costs by elementary function integrated. So far, this considerable growth of the semiconductor industry has been due to its technological capability to constantly miniaturize the elementary components of circuits, namely the MOSFET (metal-oxide-semiconductor field effect transistor), the basic building block of VLSI (very large scale integration) integrated circuits. The continuous decrease of the silicon surface used by these elementary components has kept the race integration at the rhythm dictated by the famous "Moore's Law", which states that the number transistors per integrated circuit doubles every 18 to 24 months [1]. However, the conventional bulk MOSFET scaling down encountered this last decade serious physical and technological limitations, mainly related to the gate oxide (SiO_2) leakage currents [2-3], the large increase of parasitic short channel effects and the dramatic mobility reduction [4] due to highly doped silicon substrates precisely used to reduce these short channel effects. Technological solutions have been proposed in order to continue to use the "bulk solution" until the 32-28 nm ITRS nodes [5]. Most of these solutions have then introduced high-permittivity gate dielectric stacks (to reduce the gate leakage [1], [6], midgap metal gate (to suppress the Silicon gate polyde-pletion-induced parasitic capacitances) and strained silicon channel (to increase carrier mobility) [7]. However, in parallel to these efforts, alternative solutions to replace the conven-tional bulk MOSFET architecture have been proposed and studied in the recent literature. These options are numerous and can be classified in general according to three main directions: (i) the use of new materials in the continuity of the "bulk solution", allowing increasing

MOSFET performances due to their dielectric properties (permittivity), electrostatic immunity (SOI materials), mechanical (strain), or transport (mobility) properties; (ii) the complete change of the device architecture (e.g. Multiple-Gate devices, Silicon nanowires MOSFET) allowing better electrostatic control, and, as a result, intrinsic channels with higher mobilities and currents; (iii) the exploitation of certain new physical phenomena that appear at the nanometer scale, such as quantum ballistic transport, substrate orientation or modifications of the material band structure in devices/wires with nanometer dimensions [8-9].

As the MOSFET is scaling down, the sensitivity of the integrated circuits to radiation coming from the natural space or present in the terrestrial environment has been found to seriously increase [10-13]. In nowadays ultra-scaled devices, natural radiation is inducing one of the highest failure rates of all reliability concerns for devices and circuits entering in the area of nanoelectronics [5],[14]. In particular, ultra-scaled memory integrated circuits have been found to be more sensitive to single-event-upset (SEU) and digital devices more subjected to digital single-event transient (DSETs). This sensitivity is a direct consequence of the reduction of device dimensions and spacing within memory cells combined with the reduction of supply voltage and node capacitance, resulting in a decrease of both the critical charge (i.e. the minimum amount of charge required to induce the flipping of the logic state) and the sensitive area (i.e. the minimum collection area inside which a given particle can deposit enough charge to induce the flipping of the cell) [13]-[15].

As explained before, among the technological solutions to replace the bulk MOSFET, it was envisaged to completely change the device architecture, making then possible a better electrostatic control of the channel by the gate. MOSFETs designed with Double-Gate (DGFET) configuration are now widely recognized as one of the most promising solutions to meet the requirements of the roadmap at the nanometer scale [16]-[20]. These structures present a very good control of parasitic short channel effects (SCE) and drain-induced barrier lowering (DIBL) resulting from an improved electrostatic coupling between the conduction channel and the gate electrodes [20]-[22]. The constraints on the channel doping can then be greatly reduced in these devices, which can be designed with an intrinsic film. Parasitic doping level fluctuation effects are then eliminated and, in the same time, the carrier mobility and drain current are increased [23]. The intrinsic films are also characterized by a high probability of ballistic transport in the channel [24]-[28], which could additionally reinforce the electrical performances of DGFET.

Recently, a new concept of field-effect MOS transistor without junctions (called junctionless MOSFET) has been proposed [29]-[34] and experimentally validated. A junctionless MOSFET is a transistor having the same type of semiconductor throughout the entire silicon film, including the source, channel and drain regions. A Double-Gate junctionless MOSFET (JL-DGFET) contains a heavily doped silicon film sandwiched between two gate electrodes connected together. The two gates are used to deplete the silicon film (resp. to accumulate majority carriers from the doped silicon layer) and then to turn off (resp. to turn on) the device. This is a very interesting transistor, particularly from a technological point-of-view, because its fabrication is simplified compared to the conventional process (there are no doping gradients in the device [31] and no semiconductor-type inversion). The off-state current of

these devices is no longer degraded by the leakage current of the reversely-biased source-channel and channel-drain diodes, but is uniquely controlled by the gate. This could be very attractive for ultra-short devices, typically for deca-nanometer channel lengths, for which the off-state current could be reduced.

Although standard DGFETs with junctions, also called inversion-mode (IM) DGFETs, and JL-DGFETs are very similar, the operating principle of the junctionless devices is quite different from that of IM-DGFETs. The conventional IM-DGFET is normally in the off state at V_G=0 V; the source-channel and channel-drain junctions are reversely biased and the current in the transistor is off. A voltage must be applied on the gate to turn on the transistor. The vertical electric field created across the gate insulator attracts minority carriers at the silicon/insulator interface to create an inversion (conduction) channel and then these carriers flow from source to drain through this channel. Thus, in IM-DGFET transistor, the electric field is the highest when the transistor is in the on-state and the lowest in the off-state. In contrast to IM-DGFET, the electric field is high in the off-state for JL-DGFET and very low in the on-state [31]. The junctionless transistor is normally on-state and the current flows into the channel which extends throughout the entire silicon film [32]. In this transistor, the work function difference between the gate and the doped silicon film leads to a positive flat-band voltage. Therefore, in the on-state, the junctionless transistor is under flat-band conditions and the transverse electric field is zero [32]. The conduction takes place in the film volume unlike conventional devices where the conduction takes place at the silicon/insulator interface. Thus, even at high gate voltages, the majority carriers flow mainly through the film volume and not at the interface. This can be beneficial for the carrier mobility because the impact of the surface roughness is reduced. In order to switch-off the transistor, a low gate voltage has to be applied on the gates; the vertical electric field increases and depletes the film, which cuts-off the transistor (in contrast to IM-DGFET where the high electric field is used to create an inversion layer at the interface).

From a radiation-hardness point-of-view, the high doping level in the silicon film of JL-DGFET could have a negative impact on its immunity to single-events, because the floating-body effects are expected to be strong. Then, in spite of its double-gate configuration, JL-DGFET should be more sensitive to radiation than IM-DGFET where the channel is intrinsic. The transient response of the IM-DGFET devices under heavy-ion irradiation has been studied by 3-D numerical simulation in [35]-[38]. These previous studies show that IM-DGFET shows a better resistance to radiation than Fully Depleted SOI transistors (FDSOI) with single-gate, due to the enhanced control of the film potential by the two connected gates which reduces the floating-body effects. The bipolar amplification of JL-DGFET was studied in [39] and compared to that of IM-DGFET with similar geometrical parameters. In that work, we have shown that JL-DGFET is characterized by a higher bipolar gain than IM-DGFET, due to worse radiation hardness. However, in that preliminary work we have not analyzed in depth the radiation sensitivity of JL-DGFET, especially the dependence on the position of the ion strike in the channel. Similarly, the impact of time parameters of the ion track on the transient response of these devices has not been addressed.

In the present work, we investigated by 3-D numerical simulation the sensitivity to single-event of JL-DGFET and we compared the JL-DGFET behavior with that of more conventional inversion-mode devices, IM-DGFET and FDSOI. The effect of an ion strike on the main internal electrical parameters inside the structure (potential and carrier density) and on the drain current transient is investigated. JL-DGFET is compared with IM-DGFET and FDSOI in terms of collected charge and bipolar amplification. The impact on the transient response of several parameters of the ion track (such as the characteristic time and the track radius), as well as of the position of the ion strike along the channel and of the film doping level is addressed. Our simulations show that JL-DGFET may be more resistant to heavy-ion radiation (i.e. may have a lower bipolar gain) than IM-DGFET and FDSOI for some particular configurations (specific ion LET values and ion-impact locations along the channel between the source and drain contacts).

The chapter is organized as follows. In section 2 we describe in detail the simulated devices and the simulation models used in this work. The static operation of JL-DGFET, IM-DGFET and FDSOI is presented in section 3. The transient response of JL-DGFET for ions striking in the middle of the channel (at equal distance from the source and drain contacts) is detailed in section 4. In particular, we compare JL-DGFET, IM-DGFET and FDSOI in terms of electron density, electrostatic potential, drain current transient and bipolar amplification. Section 5 addresses the impact of heavy-ion track parameters (ion track characteristic time, track radius and ion strike location between source and drain contact) on the JL-DGFET transient response. The JL-DGFET behavior is systematically compared with that of IM-DGFET and FDSOI structures. Finally, section 6 presents the influence of the silicon film doping level on the bipolar amplification in JL-DGFET.

2. Simulation details

2.1. Description of the simulated devices

Figure 1 shows the schematic 3-D description of the simulated devices. Planar IM-DGFET structures are based on real devices reported in [40]. These devices are designed with 20 nm channel length, 100 nm gate width, 6 nm-thick silicon film and 1 nm-thick gate oxide. The channel is intrinsic; the source/drain regions are highly n-type doped and the doping profile in these regions is uniform. The transition between the channel and the highly–doped source/drain regions is characterized by an abrupt doping profile. JL-DGFET have the same geometrical dimensions, but the silicon film is uniformly n-type doped at 10^{19} cm^{-3}. In this device there are no highly-doped source/drain regions, as shown in Fig. 1(a). In addition, the channel thickness has to be sufficiently small in order to make possible the complete depletion of the silicon film and to be able to cut-off the device [29]. This condition is satisfied for the doping level and the film thickness considered here. The two gates are connected together in IM-DGFET and JL-DGFET. The silicon film in FDSOI devices has the same geometrical parameters and doping profiles as the silicon film of IM-DGFET. However, only a single gate controls the electrostatic potential and the current flow in the film of FDSOI. A 10 nm-thick buried oxide

and a thick silicon substrate lowly-doped at 10^{16} cm^{-3} have been also considered in FDSOI. The very thin buried oxide is necessary to minimize the short channel effects in these devices. All devices were calibrated to meet the requirements of the ITRS Low Power technology node corresponding to the year 2015 [5]. To facilitate comparison, the gates work function has been refined to achieve the same off-state current (I_{OFF}) for all devices.

2.2. Simulation models

Numerical simulations in 3 dimensions (3-D) were carried out with the DESSIS module of the commercial simulator Synopsis [41]. We considered in the simulation physical models such as Shockley-Read-Hall (SRH) and Auger recombination models, as well as the Fermi-Dirac carrier statistics. In the SRH recombination model, carrier lifetimes depend on the doping level [41-43]. The model of the effective intrinsic density includes a doping-dependent band-gap narrowing (Slotboom's model [41]) and a lattice temperature-dependent band gap. The carrier transport model used in the simulation is the hydrodynamic model which includes the energy balance equations for electrons, holes and lattice. We also used models for impact ionization and carrier mobility depending on the carrier energy calculated by the hydrodynamic model. The mobility model also takes into account the dependence of mobility with normal electric field (through the Lombardi's model [41]), temperature and channel doping. The physical parameters of the models used in the simulation (in particular the carrier mobility) are not calibrated on experimental data, but realistic values are considered in the simulation. The parameters and models chosen in this way were then used for the simulation of drain current transients induced by the energetic particle striking the sensitive area of the device. The transistors were simulated in the off-state (most sensitive case) under V_G=0 V and V_D=0.75 V.

Transient simulations have been performed considering an ion track with a Gaussian shape and a very narrow radius of 20 nm, in order to facilitate comparison with experimental and simulation results reported in references [35] and [44]. In addition, we performed in section 5.2 simulations with different track radii in order to discuss the influence of the track radius on the radiation sensitivity of the three devices simulated here. The ion track has a Gaussian time dependence centered on t=10 ps, with a characteristic time of 2 ps. We chose this characteristic time value because a good agreement was obtained in a previous study [35] between the simulation and experimental data. However, it is clear that, if we change the characteristic time of the Gaussian distribution, the transient current will be modified. Nevertheless, it is not sure that the radiation resistance of the device and its bipolar amplification will change. To clarify this point, additional simulations with different characteristic time will be presented in section 5.1. The linear energy transfer (LET) value is kept constant along the ion track; this is justified by the very short ion-track length (equal to the silicon film thickness, 6 nm).

The ion strikes the device in a vertical incidence perpendicular to the gate, as shown in Fig. 1. In a first step, we considered that the ion strikes in the middle of the channel (at equal distance from the source and drain contacts). In a second step, we will consider several locations for the ion impact between the source and the drain, in order to investigate the sensitivity of the device to the ion strike position (section 5.3). In most cases the ion track is not entirely contained in the active area of the device, which requires accurately calculating the charge deposited by
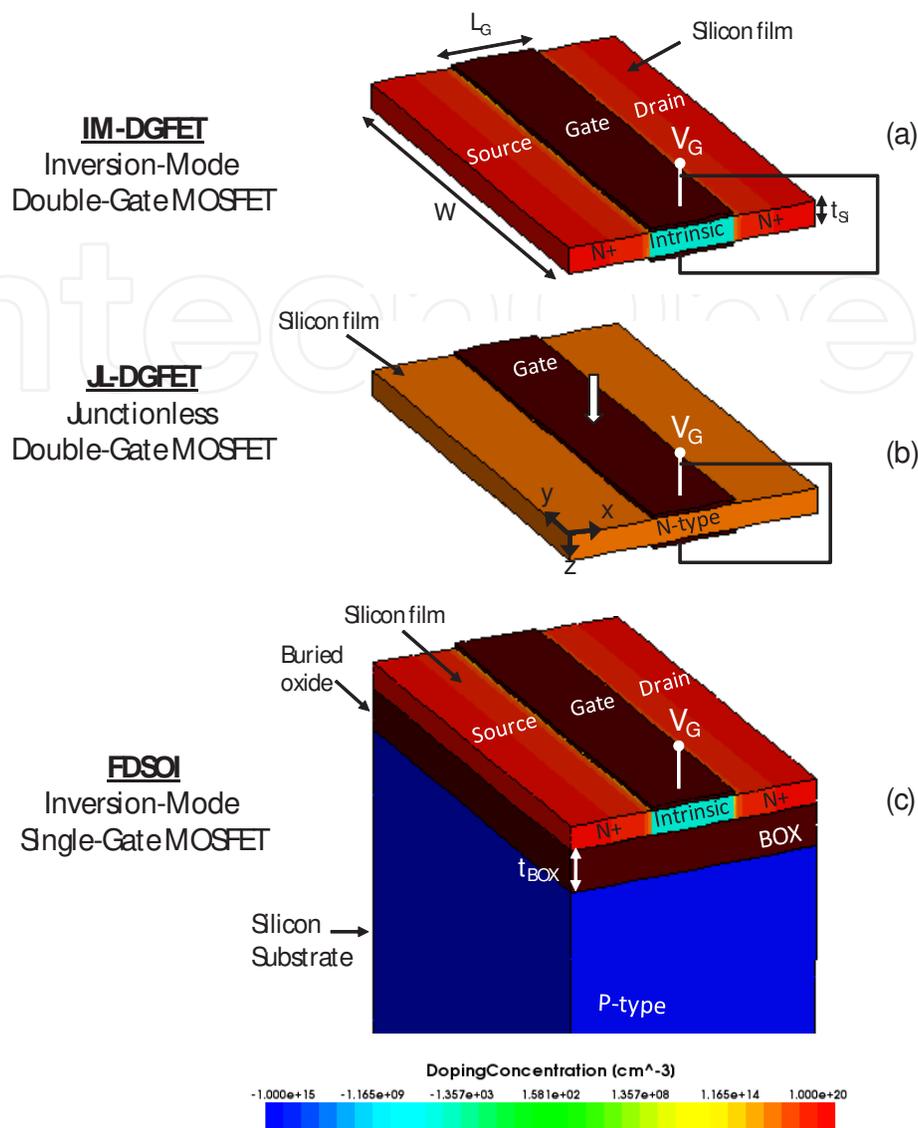
Figure 1. Schematic description of the simulated JL-DGFET (a), IM-DGFET (b), and FDSOI (c) structures considered in this work. The doping level distribution in each device is shown and the main geometrical parameters are defined. For a better view, the spacers and isolation oxide are not shown. The position of the ion strike is indicated by the arrow; the ion strikes vertically in the middle of the channel and in a direction parallel to the z axis.

the ion in the device. The deposited charge is then obtained in each case taking into account the Gaussian distribution of the ion track, the 3-D geometry of the silicon film and the exact location of the ion strike. The deposited carriers are rapidly transported (mainly by drift and diffusion mechanisms [37]) and collected by the drain contact. A part of these carriers can be recombined by carrier recombination mechanisms; the deposited charge can also be amplified by bipolar amplification mechanism. This phenomenon is specific to partially-depleted SOI (PDSOI) devices, but also exists in FDSOI [45]-[46] and double-gate transistors [37]. The charge collected at the drain contact, following the ion strike, results in a drain current transient, which is further used to accurately calculate the collected charge (by integrating the drain current on the duration of the transient). The bipolar amplification of the charge deposited by the ion is

obtained by calculating the ratio between the collected and the deposited charges. The bipolar amplification is a key-parameter that characterizes the device sensitivity to ionizing particles, and gives insights on the radiation-hardness of circuits based on this type of device.

3. Static operation

The simulated steady-state drain current characteristics of JL-DGFET, IM-DGFET and FDSOI are plotted in Fig. 2. The three devices have the same off-state current, but different subthreshold swings and on-state currents. While Double-Gate devices (both JL-DGFET and IM-DGFET) have near ideal subthreshold swings (65 mV/dec), FDSOI has a much higher subthreshold swing (90 mV/dec) because the single-gate configuration reduces the control by the gate of the channel potential and increases the parasitic short-channel effects compared to a double-gate configuration. The highest on-state current is obtained in IM-DGFET, due to the combination of a double-gate structure and an intrinsic channel; this structure has the advantage to maximize the carrier mobility. In JL-DGFET the highly-doped silicon film degrades the mobility and then, the on-state current is the lowest in spite of a double-gate configuration. The on-state current in FDSOI is situated between those of IM-DGFET and JL-DGFET: it is lower than in IM-DGFET because only a single gate controls the channel, but it is higher than in JL-DGFET since the channel is intrinsic and the mobility is enhanced.
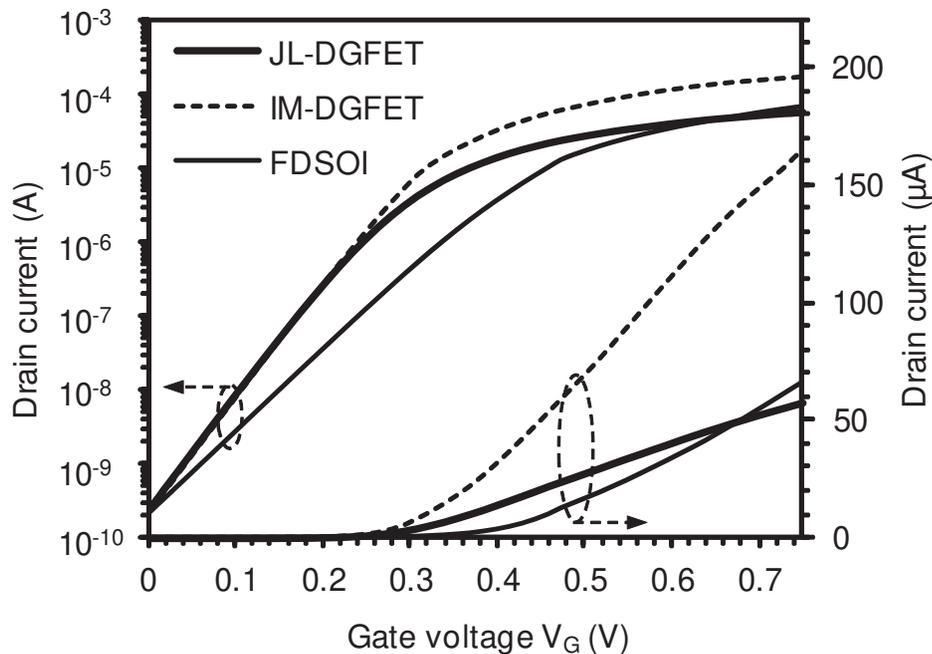

Figure 2. Drain current as a function of gate voltage for JL-DGFET, IM-DGFET and FDSOI. The gate workfunction for each device has been finely tuned to obtain the same off-state current for all devices. Characteristics simulated for V_D=0.75 V.

4. Transient operation

The 3-D distributions of the carrier density simulated before and after the ion strike are shown in Fig. 3 for JL-DGFET, IM-DGFET and FDSOI. The 2-D profile of the electrostatic in a cross-section (plane x-z in Fig. 1) corresponding to the middle of the channel is plotted in Fig. 4.
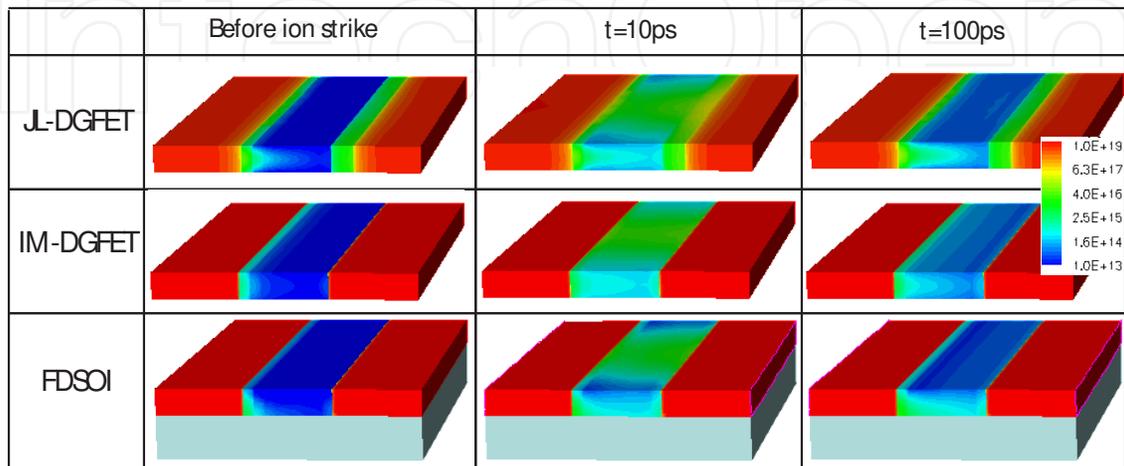

Figure 3. D profiles of electron density in JL-DGFET, IM-DGFET and FDSOI before the ion strike, at t=10 ps (maximum charge generation) and at t=100 ps. The values of the electron density are in cm^{-3}. For a better view of the film, gate material, spacers and isolation oxide are not shown. The ion strike LET is 0.1 MeV/(mg/cm^2), V_G=0 V, V_D=0.75 V.

As shown in Fig. 3, the density profiles are strongly affected by the ion strike in the three devices. As expected, the charge density on the y axis is symmetrical with respect to the middle of the film in double-gate devices and it is asymmetrical in FDSOI. At maximum deposited charge (t=10 ps), the electron density sharply increases compared to the steady state; after t=10 ps, the electron density decreases with time due to charge transport and carrier recombination mechanisms.

The ion strike not only disturbs the charge density, but also the electrostatic potential (Fig. 4) and induces a transient current which can be visualized at the drain contact. Simulated drain current transients due to the ion strike are reported in Fig. 5 for LET=0.1 MeV/(mg/cm^2). The "prompt" components of the current transients are almost identical for the three devices; on the contrary, the transient tails, representing the slow discharge component (due to floating-body effects and carrier recombination mechanisms) are very different. FDSOI shows the longest transient tail indicating the presence of stronger floating-body effects than in double-gate devices. This is confirmed by the bipolar amplification which is plotted as a function of the ion-strike LET in Fig. 6. For LET=0.1 MeV/(mg/cm^2), the bipolar gain is higher in FDSOI than in JL-DGFET and IM-DGFET. IM-DGFET shows the lowest bipolar gain owing to its double-gate configuration and its intrinsic channel. In spite of its double-gate structure, JL-DGFET has a higher bipolar gain than IM-DGFET essentially because the highly-doped silicon film enhances the floating-body effects; however, at low LET values the bipolar amplification of JL-DGFET is lower than that of single-gate FDSOI.
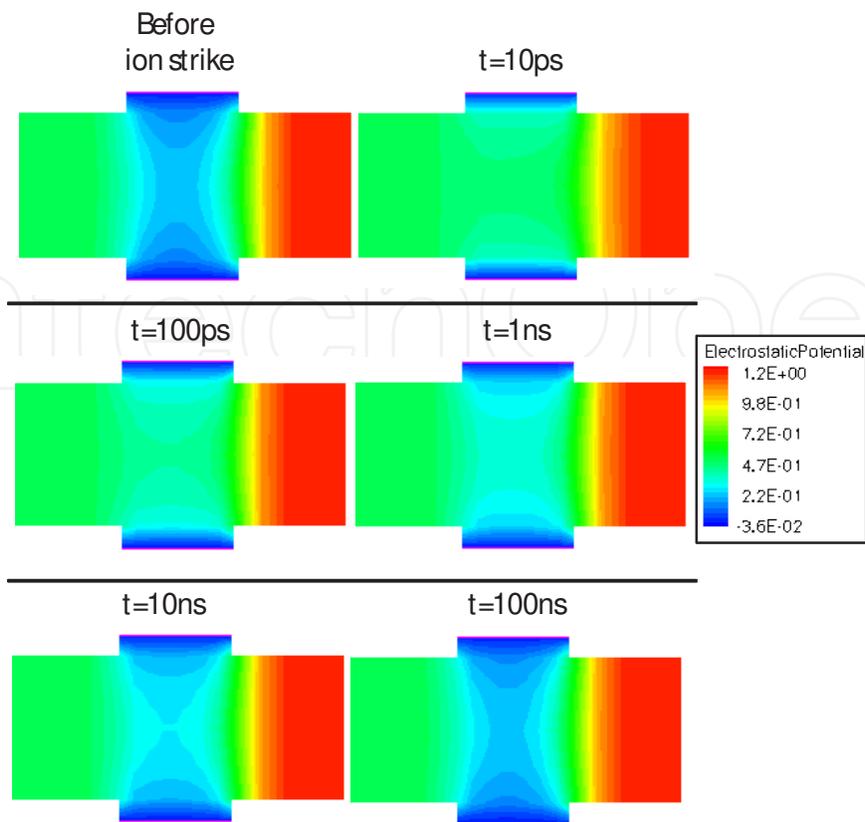
Figure 4. D profiles of the electrostatic potential (in V) within the JL-DGFET structure at different times before and after the ion strike. For a better view of the silicon film, the gate material, spacers and isolation oxide are not shown. LET=0.1 MeV/(mg/cm^2), V_G=0 V and V_D=0.75 V.
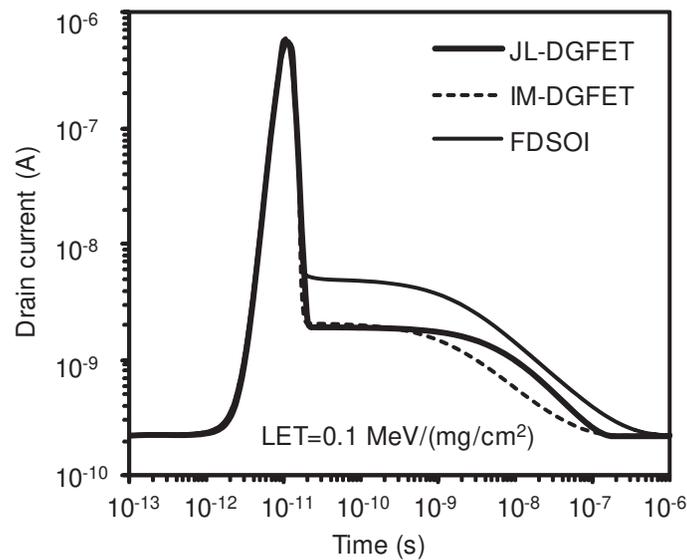

Figure 5. Drain current transients in JL-DGFET, IM-DGFET and FDSOI. All the transistors are biased in the off-state. LET=0.1 MeV/(mg/cm^2).
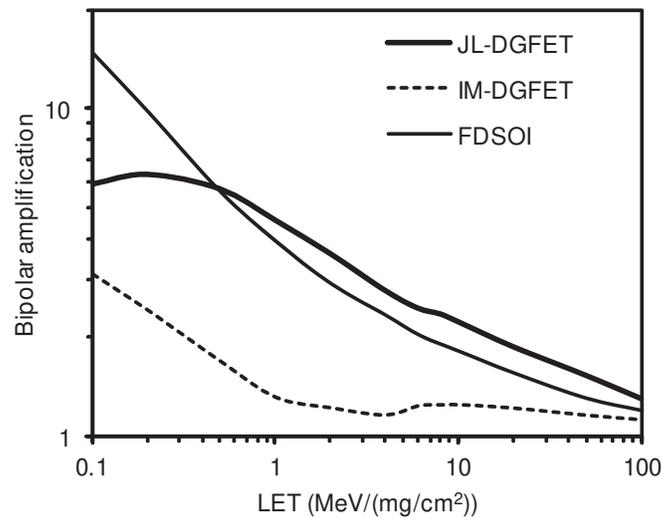
Figure 6. Bipolar gain versus the ion-strike LET in JL-DGFET, IM-DGFET and FDSOI. The ion strikes vertically in the middle of the channel between the source and drain contacts.

We recall here that in simulations presented in Fig. 6 the ion strikes the devices in the middle of the channel. We will see in section 5 that, for particular LET values, the bipolar amplification of JL-DGFET may be lower than that of IM-DGFET and FDSOI if the ion strikes the channel in other particular locations, along the x axis, between the source and drain contacts.

5. Impact of heavy-ion track parameters on the transistor transient response

In this section we study in detail the impact of several ion track parameters as well as the influence of the ion-strike location along the channel on the bipolar amplification of the three devices considered in this work. We change one parameter at a time in order to decorrelate the effects induced on the transient current and bipolar gain.

5.1. Ion track characteristic time

We begin with the characteristic time of the Gaussian time dependence of the ion track, s_hi. This parameter has a large influence on the transient current. For all previous simulations we used s_hi=2 ps since, as stated before, a very good agreement was found in a previous work between simulations and experimental data. To illustrate the impact of s_hi on the transient current and bipolar gain, we performed additional simulations with s_hi=0.5 ps. In these simulations the ion strikes in the middle of the channel and all other simulation parameters are unchanged (the same as those defined in section 2.2). Figure 7 shows the current transients obtained with s_hi=2 ps and s_hi=0.5 ps in JL-DGFET. As expected, the "prompt" component of the drain current transient is much narrower for s_hi=0.5 ps that for s_hi=2 ps. However, the transient tail is the same in both cases, which is normal, since the transient tail is essentially governed by the floating-body effects and the recombination mechanisms taking place in the device and does not depend on the time parameters of the ion track.
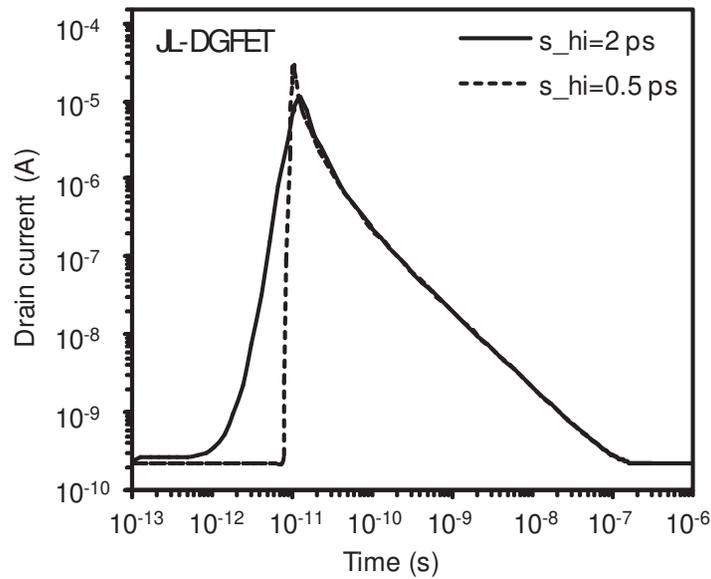
Figure 7. Drain current transients in JL-DGFET for two characteristic times of the Gaussian time dependence of the ion track. LET=1 MeV/(mg/cm²), V_G=0 V and V_D=0.75 V.

Unlike the transient current, bipolar amplification is only slightly influenced by the value of s_hi. Figure 8 shows that the gain bipolar in JL-DGFET is always higher than that of IM-DGFET (for all LET values). Compared to FDSOI, JL-DGFET is more interesting for very low LET (lower than 0.5 MeV/(mg/cm2)) where FDSOI has a stronger bipolar gain. However, for intermediate and high LET, the bipolar gain of JL-DGFET becomes slightly higher than that of FDSOI.
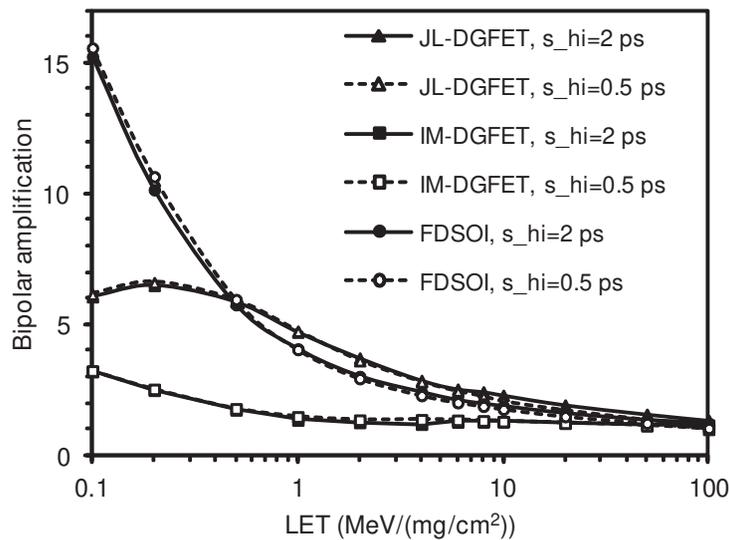

Figure 8. Bipolar amplification versus the ion-strike LET in JL-DGFET, IM-DGFET and FDSOI for two characteristic times of the Gaussian time dependence of the ion track.

5.2. Ion track radius

We have also analyzed the impact of the ion track radius on the JL-DGET transient response. For the previous analysis a very narrow (20 nm) was considered in order to facilitate the comparison with experimental and simulation results in [35] and [44]. In the following, we show simulation results performed with a larger characteristic radius r=70 nm and we compare them with results obtained at r=20 nm. The purpose of this study is to determine if the value of the ion track radius changes the conclusions regarding the increased single-event susceptibly of JL-DGFET compared to IM-DGFET. Our simulation results show that for both JL-DGFET and IM-DGFET, the current peak is higher when considering a narrow radius, mainly because more charge is deposited in the channel region of the device than in the source/drain region. This is confirmed by the collected charge which decreases when the ion track radius increases. The bipolar gain calculated for all devices considering r=70 nm is plotted in Fig. 9; results obtained for r=20 nm are also reported. Figure 9 shows that when the track radius increases the bipolar gain is only slightly modified for IM-DGFET. For JL-DGFET the bipolar gain at low LET is lower for r=70 nm than for r=20 nm, probably due to the lower deposited charge. However, at high LET the bipolar gain for r=70 nm is very similar to that obtained for r=20 nm. In spite of these variations of the collected charge and bipolar gain when the ion track radius increases, the previous trends and conclusions concerning the JL-DGFET transient response to heavy ion radiation are not changed. In the case of a larger radius the bipolar gain changes for all devices, but the bipolar amplification of JL-DGFET is still higher than that of IM-DGFET (for all LET values). These results are consistent with simulation data obtained in [39]. Compared to FDSOI, the bipolar amplification of JL-DGFET is weaker for LET values less than 1 MeV/(mg/cm^2), and becomes slightly higher for LET>1 MeV/(mg/cm^2).
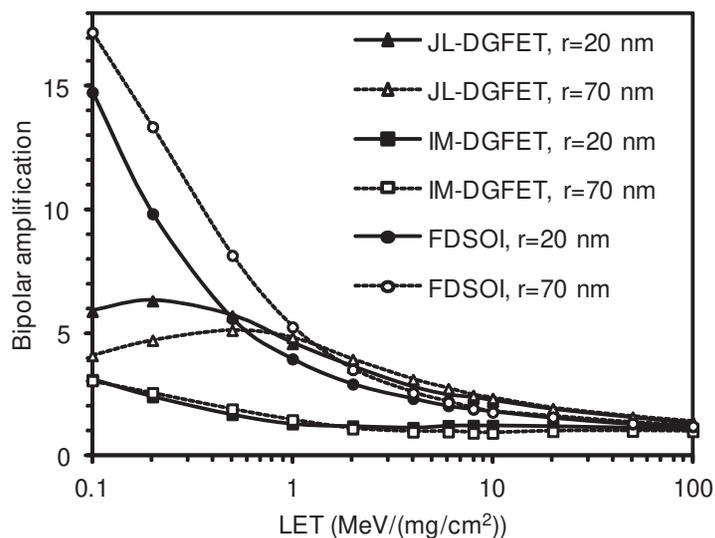

Figure 9. Bipolar amplification versus the ion-strike LET in JL-DGFET, IM-DGFET and FDSOI for two radii of the ion track. V_G=0 V and V_D=0.75 V.

5.3. Ion strike location between source and drain contacts

Until now we have considered that the ion hits the device in the middle of the channel. In this part we are changing the location of the ion strike along the channel (x-axis) in order to study the impact of this position on the radiation sensitivity of JL-DGFET compared to that of IM-DGFET and FDSOI. In the following, the track radius is 20 nm, s_hi=2 ps and all other parameters are those defined in section 2.2. Several locations of ion strike are considered between the source contact (x=0) and the drain contact (x=60 nm), as shown in Fig. 10.

The 3-D profile of the heavy-ion charge density in the entire silicon film (the same for all three devices) is shown in this figure for an ion strike in x=10 nm. For this particular location, as shown in Fig. 10, the ion track is not entirely contained on the silicon film. This is also the case for other locations, which requires a specific calculation of the deposited charge. For each location, the current transient is simulated and the collected charge is extracted from this transient. Finally, the bipolar gain is calculated at a given LET for each x value.
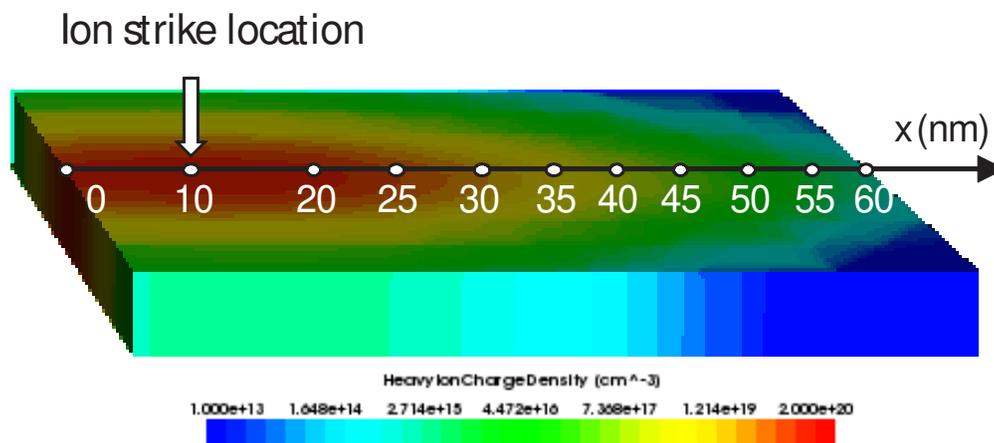

Figure 10. D profiles of the heavy-ion charge density in the silicon film of JL-DGFET for an ion strike at x=10 nm and LET=2 MeV/(mg/cm²). The values of the heavy-ion charge density are in cm⁻³. For a better view of the film, gate material, spacers and isolation oxide are not shown. The position of the ion strike is indicated by the arrow. Other positions for the ion strike considered in this work are also indicated.

For simulations considering the ion strike in the middle of the channel (x=30 nm), we saw that JL-DGFET always shows a higher bipolar gain than IM-DGFET (for all LET values). In addition, the bipolar gain of JL-DGFET is also higher than that of FDSOI for intermediate and high LET. The purpose of this section is to verify whether these conclusions also apply to other locations of the ion strike along the channel. The collected charge as a function of the x location is shown in Fig. 11 for both very low and very high LET values. The deposited charge, calculated for each x location and each LET, is also reported in this figure to facilitate the comparison. The deposited charge is maximum in the middle of the channel and decreases towards the sides of the silicon film, because a smaller part of ion track is contained in the active region when the ion strike position moves towards the source or drain contacts. At very low LET=0.2 MeV/ (mg/cm²) and for all x locations, the lowest collected charge is obtained for IM-DGFET and the

highest collected charge for FDSOI (Fig. 11(a)). This result shows that the trend obtained for x=30 nm is confirmed for all other locations. For all devices, the collected charge has a bell-shaped profile with a maximum around the middle of the channel (where the deposited charge is the highest) and two minima at the source and drain contacts (where the deposited charge is the lowest). The collected charge is always higher than the deposited charge for all x locations, which indicates a strong bipolar amplification. The behavior is quite different for LET=80 MeV/(mg/cm²), as shown in Fig. 11(b). For ion strikes located between the source contact and the middle of the channel, the collected charge is higher for JL-DGFET than that of FDSOI and IM-DGFET. It is also interesting to note that for x locations situated between the source contact (x=0) and the middle of the channel, the collected charge is lower than the deposited charge. This indicates that the bipolar amplification is very low and there is a strong recombination of the deposited charge in the device. Beyond x=30 nm, the collected charge for JL-DGFET decreases and becomes lower than that of IM-DGFET and FDSOI. These results show that for a high LET, the trends obtained for ion strikes in the middle of the channel are no longer valid for ion strikes located in the vicinity of the drain region, beyond x=30 nm. In addition, these results show, for the first time, that JL-DGFET is able to collect a smaller amount of charge than IM-DGFET for these specific values of x location and LET.
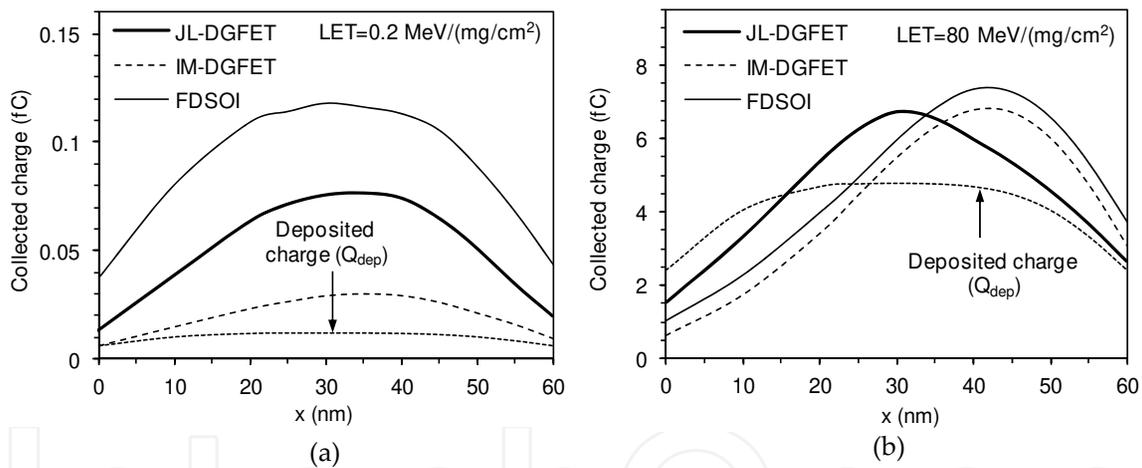

Figure 11. Collected charge as function of the x location in IM-DGFET, JL-DGFET and FDSOI. The deposited charge is also plotted for comparison. (a) LET=0.2 MeV/(mg/cm²) and (b) LET=80 MeV/(mg/cm²).

To confirm these new findings and highlight the range of LET for which these observations are valid, we calculated the bipolar gain as a function of x for different LET values. Figure 12(a) shows, as expected, that at LET=0.2 MeV/(mg/cm²) the bipolar gain of FDSOI is the highest and the gain of JL-DGFET is situated between that of FDSOI and IM-DGFET. JL-DGFET is therefore more resistant to radiations than FDSOI, but IM-DGFET remains the most interesting device for low LET. This trend continues when LET increases until LET values around 0.5 MeV/(mg/cm²). For LET values between 0.5 MeV/(mg/cm²) and 20 MeV/(mg/cm²) (approximately), JL-DGFET shows the highest bipolar gain for all x locations, IM-DGFET always having the lowest gain. The bipolar gain of JL-DGFET is slightly higher than that of FDSOI for x locations

beyond 40 nm. The trend changes for LET values above 20 MeV/(mg/cm^2). This can be visualized in Fig. 12(b) which shows the bipolar amplification for LET=30 MeV/(mg/cm^2). Finally, Fig. 13 shows the bipolar amplification as a function of x location for LET=80 MeV/(mg/cm^2). Although for x less than 30 nm IM-DGFET remains the most interesting device in terms of radiation resistance, for x location beyond about 30 nm, the bipolar gain of JL-DGFET becomes the lowest.
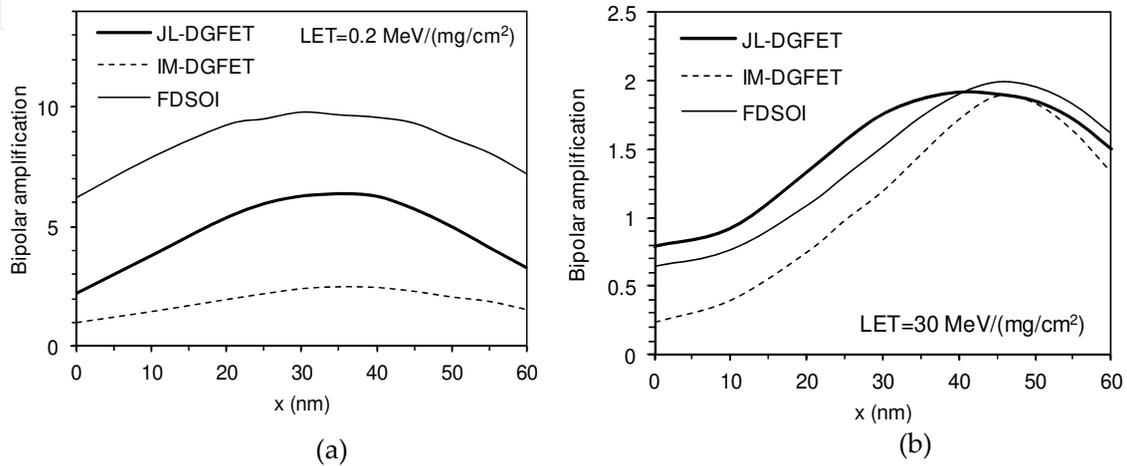

Figure 12. Bipolar amplification as a function of the x position of the ion strike in JL-DGFET, IM-DGFET and FDSOI for (a) LET=0.2 MeV/(mg/cm^2) and (b) LET=30 MeV/(mg/cm^2).
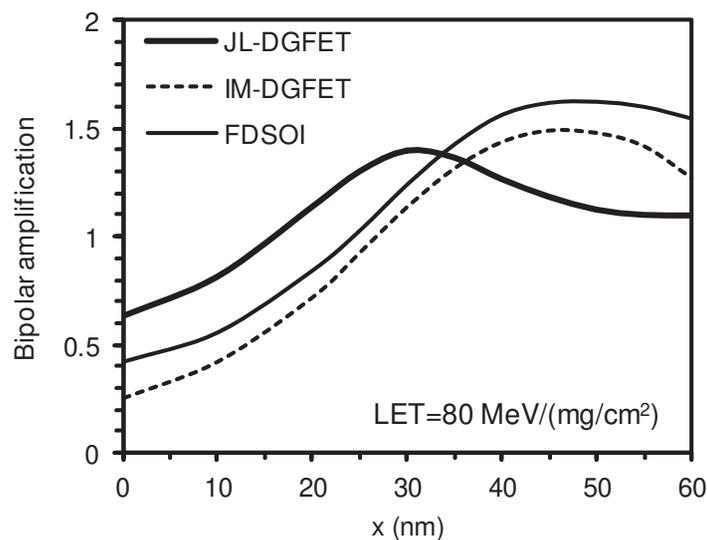

Figure 13. Bipolar amplification as a function of the x position of the ion strike in JL-DGFET, IM-DGFET and FDSOI for LET=80 MeV/(mg/cm^2).

We summarize these results in Table 1, indicating for each range of values the device having the lowest bipolar gain:

a. for ion strike locations in the first part of the channel (between the source contact and the middle of the channel) IM-DGFET has the lowest bipolar amplification for all LET values.

b. for x locations beyond the middle of the channel:

- for LET<20 MeV/(mg/cm^2), the bipolar gain of IM-DGFET is always the smallest.

- for LET>20 MeV/(mg/cm^2), JL-DGFET has the lowest bipolar gain; the JL-DGFET becomes more resistant to radiation than IM-DGFET and FDSOI.

In addition, compared to FDSOI, JL-DGFET is also more resistant to radiation for LET<0.5 MeV/(mg/cm^2) and all x locations. These results show that there are LET ranges and specific ion-strike locations for which JL-DGFET can be more interesting in terms of radiation hardness than more conventional inversion-mode devices such as FDSOI and IM-DGFET.

Ion strike location x	LET values	Lowest bipolar gain
Between source contact and middle of the channel	All LET values	IM-DGFET
Beyond the middle of the channel	< 20 MeV/(mg/cm^2)	IM-DGFET
	> 20 MeV/(mg/cm^2)	JL-DGFET

Table 1. Simulation results summary indicating the device characterized by the lowest bipolar gain as function of the ion strike location and LET values.

Finally, we compared our results with experimental and simulation results published in Ref. [35]; the purpose is to validate a part of our previous results showing that JL-DGFET could have a lower radiation sensitivity than inversion-mode devices such as IM-DGFET and FDSOI for ion strikes near the drain and ion LET values higher than 20 MeV/(mg/cm^2). In [35] we investigated the transient response of inversion-mode FD single-gate SOI MOSFET designed with 80 and 50 nm gate length, 11 nm-thick silicon film and intrinsic channel. In that work we found an excellent agreement between experimental bipolar gain values (measured by heavy ions experiments) and simulated bipolar gain obtained with 3-D numerical simulation. The results were also consistent with experimental data obtained by pulsed laser irradiation performed on 80 nm gate length FD SOI MOSFETs fabricated with the same technology [44]. In [35] the ion strikes in a location situated in the drain region, location equivalent to x=50 nm in the present work. For this reason, we plot in Fig. 14, the bipolar gain for JL-DGFET, IM-DGFET and FDSOI for a ion strike at x=50 nm and ion LET values between 10 and 100 MeV/(mg/cm^2). The experimental and simulation data from [35] are also reported in Fig. 14. This figure indicates that the bipolar gain in JL-DGFET is lower than the experimental and simulated bipolar gain in FD SOI 80 nm and FD SOI 50 nm. The comparison is not easy because the silicon film thickness and the channel length are not the same in JL-DGFET and FD SOI devices measured in [35]. However, these experimental data confirm our simulation results

concerning JL-DGFET, which shows lower bipolar amplification than IM-DGFET and FDSOI for ion strikes near the drain and ion LET values higher than 20 MeV/(mg/cm^2).
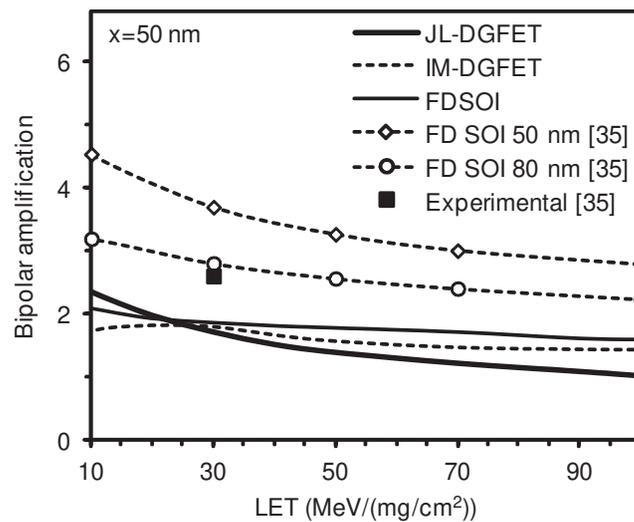

Figure 14. Bipolar amplification vs. LET in JL-DGFET, IM-DGFET and FDSOI for an ion strike at x=50 nm and comparison with experimental and simulated data obtained in [35] for FD SOI MOSFET.

6. Impact of film doping level on the JL-DGFET transient response

For JL-DGFET, we also investigated the impact of channel doping level on the drain current transient and bipolar amplification. Three channel doping levels have been considered in simulation: 1×10^{19}, 2×10^{19} and 3×10^{19} cm^{-3}. In JL-DGFET the channel thickness has to be sufficiently small in order to be able to fully deplete the channel of carriers and to turn the device off [29]. The higher the channel doping level, the smaller the film thickness needs to be. This condition is satisfied for all the doping levels and the film thickness considered here. All devices have been calibrated to fill the ITRS Low-Power requirements for the technology node corresponding to the year 2015 [5]. In order to facilitate the comparison, the gate work-function has been finely tuned to obtain the same off-state current (I_{OFF}) for all devices.

When the channel doping increase, the floating body effects are enhanced and the drain current transient is longer, as shown in Fig. 15. Both the collected charge (Fig. 16) and bipolar amplification (Fig. 17) increase with the channel doping. Impact ionization is also larger for higher doping levels, which additionally contribute to enhance the bipolar amplification. Very high values of the bipolar gain are found for a channel doping of 3×10^{19} cm^{-3}, but these values are reduced when a larger ion track radius is considered in simulation. Finally, at very high LET the electric field collapses and the bipolar gain decreases below 2.5 for all devices.
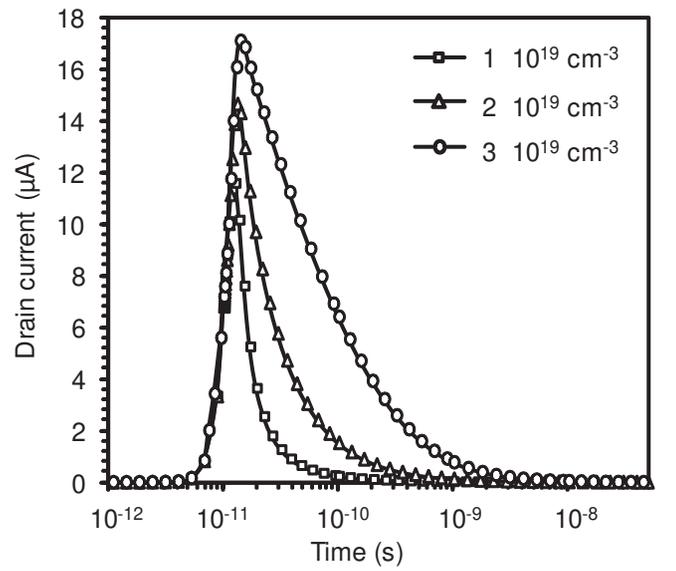
Figure 15. Drain current transient in JL-DGFET for different film doping levels. The incident ion LET is 1 MeV/(mg/cm^2). V_G=0 V and V_D=0.75 V.

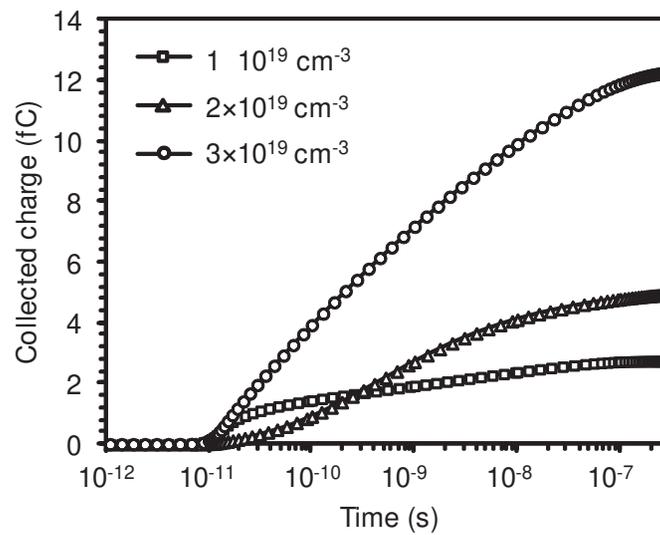**Figure 16.** Collected charge in JL-DGFET for different film doping levels. The incident ion LET is 1 MeV/(mg/cm^2). V_G=0 V and V_D=0.75 V.
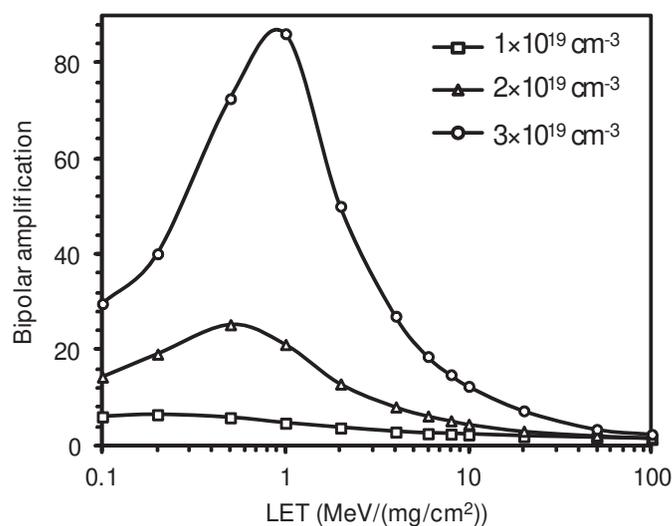
Figure 17. Bipolar amplification as function of LET in JL-DGFET for different film doping levels. V_G=0 V and V_D=0.75 V.

7. Conclusion

In conclusion, this chapter presented a detailed investigation of the radiation sensitivity of JL-DGFET by 3-D numerical simulation. In particular, the bipolar gain of JL-DGFET has been compared with that of more conventional inversion-mode devices such as FDSOI and IM-DGFET. We have firstly shown that for an ion strike in the middle of the channel, IM-DGFET shows a lower bipolar gain than JL-DGFET and FDSOI (for all LET values). We also studied the impact of various parameters of the ion track (characteristic time and track radius) on the drain current transient and bipolar gain of JL-DGFET. Our results show that modifying these parameters does not change the previous conclusion, the bipolar gain of IM-DGFET being always smaller than those of JL-DGFET and FDSOI. However, a thorough study of the bipolar gain as a function of the ion strike position along the channel showed that JL-DGFET has a lower bipolar gain than IM-DGFET and FDSOI for some particular conditions, precisely for LET values superior to 20 MeV/(mg/cm²) and ion strike positions between the middle of the channel and the drain contact. These results are also confirmed by already published experimental and simulation data obtained on FD SOI MOSFETs with longer channels. JL-DGFET is also better than FDSOI for low LET values below 0.5 MeV/(mg/cm²) (for all ion strike positions).

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