10

Non-Volatile Memory Devices Based on Chalcogenide Materials

Fei Wang
California State University, Long Beach,
United States of America

1. Introduction

Non-volatile memory refers to memory devices that can retain stored information even when electric power is not applied. Usually, non-volatile memories are utilized as secondary storage in computers, long term persistent storage and portable data storage. The most popular portable non-volatile memory nowadays is the Flash memory. The common device structure of a flash memory cell contains a MOSFET with a floating gate. The information storage relies on charge storage on the floating gate. Currently, there exist two types of flash technology: NOR and NAND technology. NAND technology tends to dominate because of its better scaling potential and lower cost. The major concerns regarding the floating gate based flash memory now is its scaling limitations. Challenges, such as cell-to-cell interference and programming disturbance, require closer attention, especially for short gated devices. Solutions have been researched in both software development for flash memory, such as sophisticated reading/writing controller, and physical structure improvement. Nano-floating gate structure is one of the proposed physical solutions to overcome the scaling challenges of flash memory [38]. Instead of using a floating gate, this new proposed structure uses silicon nanocrystals to trap charges. This structure can be used to build devices with much thinner oxide layer, which reduces the size. However, concerns still exist about its data retention capabilities.

Moreover, the current prevailing writing operation for flash memory is called block writing, which includes four steps: 1) Dump the whole block into a buffer DRAM; 2) Write new information into DRAM; 3) Erase old information in Flash; 4) Write information stored in DRAM into Flash. This requirement on buffer DRAM adds complexity to flash memory, which results in more chip space occupation and lower speed.

As the demand for data storage capability increases, memory density and reading/writing speed have become key factors for technology advancement. To overcome or compensate the limitations of flash memory technology, innovative concepts and materials are being investigated. Non-volatile memory devices based on chalcogenide materials are the most promising technology due to its fast reading/writing speed and high scalability. In addition to those, since the information storage for chalcogenide devices are based on phase or electrochemical reaction, chalcogenide based devices display excellent retention characteristic, especially so when compared to flash memories that rely on charge storage.

In general, information storage devices based on chalcogenide materials could be categorized into two types. Phase change memory (PCM) is one of them. The information storage is realized by converting nanoscale grains of chalcogenide materials between an amorphous state and a crystalline state [1]. The conversion requires applying heat onto nanoscale memory grain. This can be done through either optical or electrical methods. Optical phase change memory was developed and commercialized in 1990s. Now it is widely used in rewritable optical data recording (e.g. RW-DVD discs). Electronic phase change memory did not attract much attention at the beginning, mainly due to the vast developemnt of charge-storage memories, such as EPROM and Flash. Not until the recent decade, when scaling limitation raise concerns on charge-storage memories, does electronic PCM re-gain attention of the memory industry. Materials used as active recording layers for PCM are Sb-Te containing alloys, with the most widely used material being the Ge-Sb-Te (GST) system [2-4].
The other type of information storage mechanism is relatively new. It is known as Programmable Metallization Cell memory (PMC). This type of memory device relocates metal ions in a solid state electrolyte using electrochemical methods [5-6]. Therefore, one can control the resistivity of the solid state electrolyte to achieve the data recording purpose. The PMC was first suggested by M. Kozicki [5] in early 2000s. Several research groups and indutrial R&D are inverstigating in this direction now. A variety of names have been given to this type of devices, such as conductive-bridge RAM, nanobridge memory and eletrolytic memory etc. Materials used as active recording films for this category are metal containing chacogenides, such as Ag-Se, Ag-S [7], Ag-Ge-Se [5-6], Ag-Ge-S [8], Cu-S [9] etc. PMC, compared to PCM, has the advantages in terms of short recording time, low recording power as well as better scaling capability [5-6].

2. Chalcogenide materials

Chalcogenide materials used in both PCM and PMC are usually in glassy form. Glass is also called amorphous materials or disordered materials. Not like crystals, glassy materials do not have long range order in their lattice. This kind of disordered structure makes possible some unique properties of glassy materials. Chalcogenide glasses are simply glasses containing elements from group VI of periodic table; usually they are alloys of group IV and/or group V elements together with group VI elements. When heated, solid glass experience three critical temperatures (Fig 1): glass transition temperature (T_g), crystallization temperature (T_c) and melting temperature (T_m). Glass transition temperature is a signature of significant softening of glasses; it is measured by probing the viscosity of glasses. Glasses with temperature above T_g but below T_m are still in solid format, but with lower viscosity. This is significantly different from crystals, which do not have T_g. When temperature increases up to T_c, glasses starts to crystallize, results in poly-crystal in most situations. Increasing temperature above T_m will melt the glasses. Genrallay, crystallizaon process has two states, nucleation state and crystal growth state. At crsystallization temperature, molecules starts to gather into clusters, thus forms nuclei. The crystal will further grow from those nuclei. The crystal growth process needs time, which is material dependent. Glasses are usually obtained by quickly quenching melts. This quenching process forces temperature to by-pass T_c quickly, so that crystallization does not have time to happen. The GST system (Ge-Sb-Te) used in PCM devices has a typical melting temperature of 600^{o}C, and its crystalization temperature is between 100-150^{o}C depend on specific chemical composition.

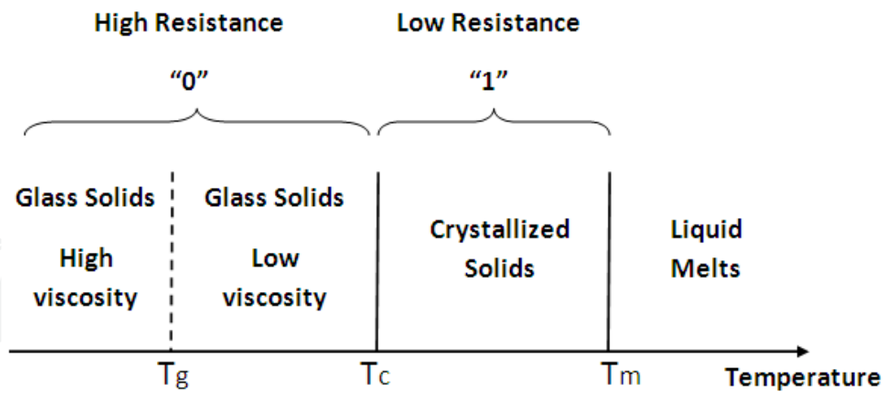


Fig. 1. Phase changes of glassy materials as a function of temperature. Three critical temperatures are observed: glass transition temperature (T_g), crystallization temperature (T_c) and melting temperature (T_m).

Not all compositions can form glasses; some compositions tend to crystallize easily during quenching, those compositions are called poor glass formers. Application of chalcogenide glasses requires their glassy state to be stable, i.e. good glass formers. Boolchand *et. al.* suggested that chalcogenide glasses display three elastic phases as a function of their mean coordination number: floppy phase, Intermediate phase (IP) and stressed rigid phase (Fig 2) [10-22]. Glass compositions in floppy phase and stressed rigid phase are usually poor glass formers due to the high internal stress in their molecular structure. Compositions in IP are usually good glass formers because their molecular networks are nearly stress free. Good glass formers are needed for PCM devices since they can form glass even when temperature is brought down slowly. Therefore, compositions in IP are ideal for PCM devices. Within the glass forming region of Ge-Sb-Te system, increasing composition of Ge usually increases the melting temperature, which is undesireable because of the power concerns. On the other hand, decreasing the Ge content will cause the glass become unstable in glassy states, which causes problem in term of data retention. Therefore, typical compositions selected for PCM

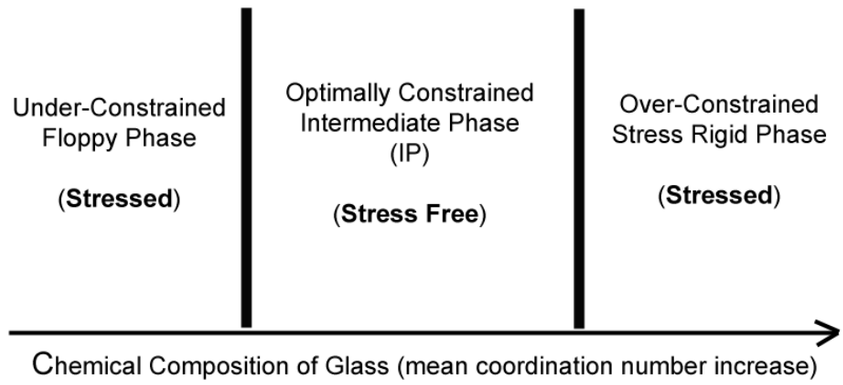


Fig. 2. Elastic phases in chalcogenide glasses as a function of mean coordination number of glasses. Mean coordination number is an indicator of chemical composition.

devices is $Ge_2Sb_2Te_5$ system (GST-225). The GST-225 system have typical melting temperature of 600°C, and its crystalization temperature is around 120°C. Glasses in IP are also ideal for PMC devices. The stress free nature of their network structure makes them good solid state solvent for metal additives, which is necessary for PMC devices.

3. Phase Change Memory (PCM)

3.1 Theoretical background

The operation of PCM devices relies on the resistance difference between the glassy phase (amorphous phase) and the crystalline phase. The materials used in PCM are mostly Tellurium based glasses, i.e. GST systems. As shown in Fig. 1, amorphous phase usually displays high resistance, which corresponds to logic '0'; crystalline phase usually displays lower resistance, which corresponds to logic '1'. The typical high resistance, i.e. Off resistance, is in 10^6 Ω range, and the typical low resistance, i.e. On resistance, is in 10^3 Ω range.

In order to convert the active material from amorphous phase (logic '0') to crystalline phase (logic '1'), one needs to increase the cell temperature above T_c, but below T_m. This corresponds to the SET process in logic memory. However, crystallization process needs time. Depends on the size of the cell, it may take 100~500ns. This somewhat limits the speeds of PCM memory. On the other hand, to convert from crystalline phase to amorphous phase, one needs to increase temperature to a higher level, all the way up to above T_m. Once the cell melts, remove heat and let the cell quench. The cell then returns to amorphous phase, i.e. logic '0'. This process corresponds to the RESET process.

Fig. 3 shows the SET and RESET process of PCM cell. The heating is controlled by cell current. During SET process, cell current is controlled in SET region, this assures the cell temperature is between T_c and T_m. During RESET process, cell current is much higher, at least above I_{RESET_min}, this assures cell temperature is high enough to form melts.

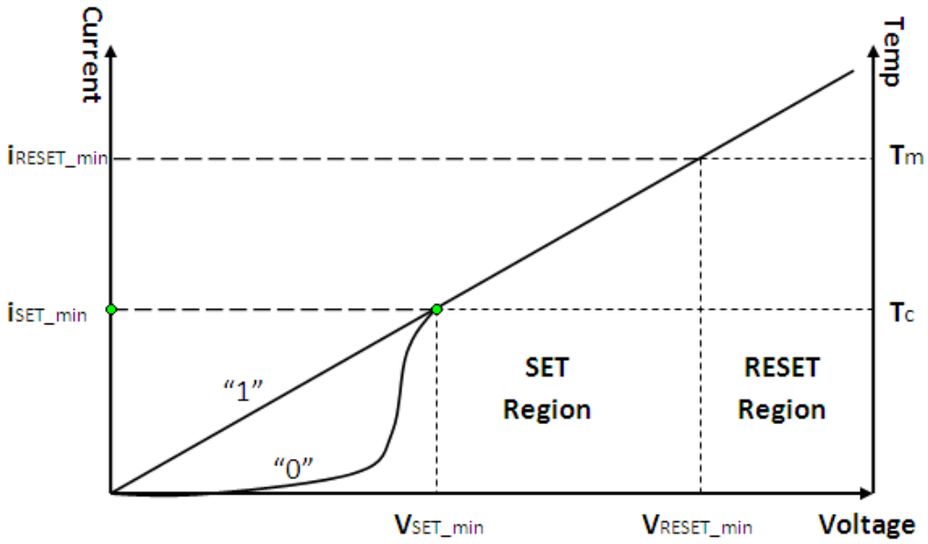


Fig. 3. SET and RESET process of PCM cell. PCM cell temperature is controlled by cell current. i_{SET_min} corresponds to crystallization temperature T_c; i_{RESET_min} corresponds to melting temperature T_m.

3.2 Device structure

Fig. 4 shows a typical structure of a vertical PCM cell. This figure is taken from Woo Yeong Cho et. al.'s IEEE contribution [23]. A PCM cell is composed of an access transistor and an active element, which is usually GST material sandwiched between two electrodes. The gate of the access transistor is controlled by word line. The top electrode (TE) is connected to bit line. Only when both bit line and word line are active, this PCM cell is selected, i.e. current is allowed. In order to improve the heating efficiency, The bottom electrode (BE) is in contact of GST material through a narrow bottom electrode contact (BEC). This BEC structure increases the current density of the cell, therefore, the heating efficiency as well.

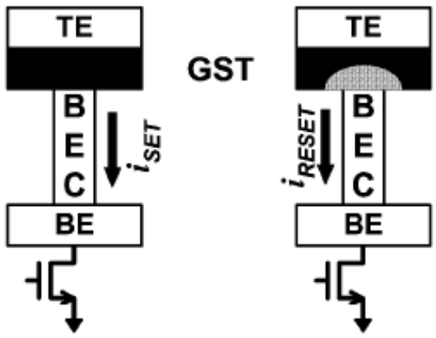


Fig. 4. Typical structure of PCM cell. Left picture indicates a cell during SET process; Right picture indicates a cell during RESET process. Top electrode (TE) is connected to bit line, while the gate of access transistor is connected to word line. [23]

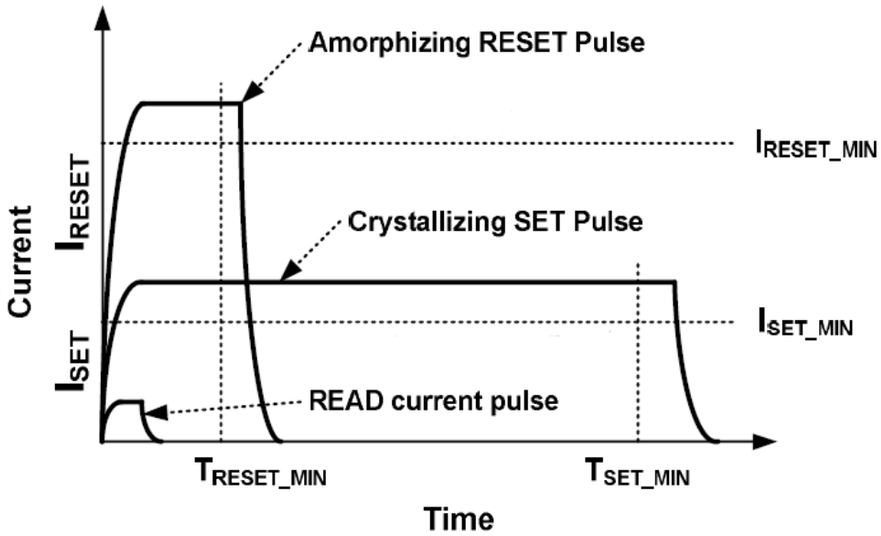


Fig. 5. Current pulses used in reading, SET and RESET processes. [24]

3.3 Reading and writing process

Fig. 5 shows the basic reading and writing process of PCM cell. This figure is taken from Byung-Do Yang et. al.'s IEEE contribution [24]. Writing has two different processes, SET

(writing logic '1') and RESET (writing logic '0'). As mentioned earlier, SET process needs lower writing current, but longer time. On the contrary, RESET process needs higher writing current but shorter duration. This is because melting is an instantaneous phase change, but crystallization is a gradual process. Typical SET time is 100~500ns, while typical RESET time is 50-100ns, depends on the size of the device.

Reading is actually a sensing process. During reading process, the phase of active material cannot be affected. Therefore, reading current is much lower than the I_{SET_min}. This assures the cell temperature is always lower than T_c during reading process; therefore, the cell resistance remains in its original category. Typical reading time is around 50ns.

The detailed programming steps are explained as the following [23-24]:

1. RESET

A high voltage is applied on the bit line (BL), while the word line (WL) is active for 50~100ns so that the access transistor is ON during RESET time. This high voltage generate high current, which will melt the GST material. Once RESET time elapses, the current is removed abruptly by de-activate WL. This forces GST material to cool rapidly, hence turns into glass.

2. SET

A medium voltage is applied on BL, while the WL is active for 100~500ns so that the access transistor is ON during SET time. This voltage is not so high to melt the GST material, but is enough to heat it above crystallization temperature (T_c). During SET time, small crystal nucleus form firstly, then grow into larger crystalline structures. Once SET time elapses, heat is removed, proper crystalline phase is formed.

3. READ

A low voltage is applied on BL, while WL is active to turn on access transistor during read time. The stored data is sensed by comparing the BL current with a reference value. If BL current is higher than reference, a logic '1' is identified; if BL current is lower than reference, a logic '0' is identified.

As we mentioned earlier, the programming process of PCM cells heavily relies on resistive heating by elevated currents. This requires the adjacent PCM cells to be isolated properly. Otherwise, disturbances in un-selected cells may cause unwanted writing. On the other hand, reading, SET and RESET current/voltage needs to be carefully calibrated to guarantee 1) they are within design limits; 2) within current/voltage rating of the device.

3.4 Current development in the field

The most widely used information storage media for Phase Change Memory now is $Ge_2Sb_2Te_5$ (GST). Nevertheless, concerns regarding the high SET/RESET threshold and low SET speed of GST material stimulate the efforts in seeking new phase change materials. S. Song et al. [28] recently reported the potential of a low power phase change application using Sb_2Te_3-Ta_2O_5. They claim that the above mentioned material can achieve phase change with lower RESET threshold and shorter pulse width. With a pulse width of 100ns, the RESET threshold is 1.6V, compared to 4.0V for single-layer GST device. This reduction in RESET voltage is due to two factors: 1) The reduced thermal conductivity of Sb_2Te_3-$Ta2O_5$, which is 0.46W/mK compared to 0.54W/mK of crystalline GST. This leads to efficient Joule heating, thereby reducing the voltage required to amorphorize; 2) The lower melting point of Sb_2Te_3-Ta_2O_5 compared to GST. They also found that the Sb_2Te_3-Ta_2O_5 based device could achieve fast programming with pulse width as short as 20ns.

In addition, binary $Sb_{80}Te_{20}$ material is also found to display desirable properties, such as low threshold and fast SET speed. The problem with the pure binary $Sb_{80}Te_{20}$ is its low crystallization temperature, which would be a stability concern. Research has been devoted into doping materials into $Sb_{80}Te_{20}$ [29] or forming a multilayer structure [30] to overcome this issue. Wang et al. [31] recently reported a nano-composite multilayer structure incorporating $Sb_{80}Te_{20}$ and the dielectric material SiO_2. They found by tuning the thickness of $Sb_{80}Te_{20}$ film with respect to SiO_2 layer, one can tune the crystallization temperature, making it higher than that of pure $Sb_{80}Te_{20}$.

With the purpose of increasing the data storage density, research has also been devoted into seeking multi-level storage using a single cell. Y. Gu et al. [32] recently reported that by adjusting the composition of Ge-Sb-Te, one can achieve 3 distinct resistance level by carefully controlling the SET current. They found that $Ge_{15}Sb_{85}Se_{0.8}$ composition display a first resistance shift from $1x10^4$ Ω to $5x10^3$ Ω at 528K and a second resistance shift from $5x10^3$ Ω to $1x10^2$ Ω at 602K. This indicates the possibility to store more than 1 bit of information in the same cell. Y. Yin and S. Hosaka [33] also reported multi-level storage using SbTeN materials. They proved that a 2 bits storage is feasible using the above mentioned material, as shown in Fig. 6. According to their experiment, the SET from R0 to R1 needs 0.4 mA, SET from R1 to R2 needs 0.8 mA, while SET from R2-R3 needs 1.2 mA. The spaces between SET current thresholds are pretty large, so that the manipulation is not hard.

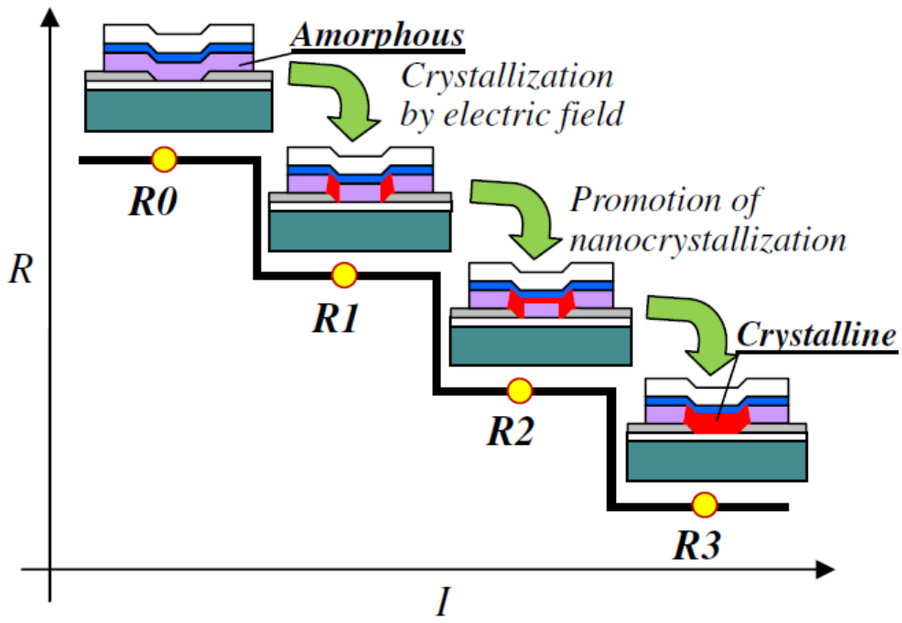


Fig. 6. Multi-level resistance based on promotion of nano-crystallization with programming currents [33]

4. Programmable Metallization Cell (PMC)

4.1 Theoretical background

Active materials forming PMC cells are called solid state electrolytes. They are named so because they are somewhat analogous to liquid state electrolytes. We all know that in liquid electrolytes, ions' mobility is high enough to serve as current carriers. Similarly, solid state

electrolyte also contains ions that are highly movable, majorly they are metal ions that carry positive charges. Many materials can serve as solid state electrolytes. Basically, they can be categorized into two types, chalcogenide-based electrolytes (Ag-Se/S, Cu-Se/S, Ag-Ge-Se/S, Cu-Ge-Se/S [5-9]etc.) and oxide-based electrolytes (WO_3) [25]. We will focus on chalcogenide based electrolytes in this paper.

The process of PMC operation is actually an electro-chemical process. A simple PMC cell is just a thin layer of solid state electrolyte sandwiched between an anode and a cathode. Anode is an electrode that serves as a source of metal ions in active layers. For example, if the solid state electrolyte is silver (Ag) based, i.e. Ag-Se or Ag-Ge-Se, the anode must be Ag. Cathode is an inert electrode, such as nickel (Ni) or aluminum (Al).

A forward voltage bias across the PMC cell will cause the metal ions move towards cathode and eventually be oxidized into metal atoms. Oxidized metal atoms accumulate on cathode, growing towards anode. On the other hand, metal atoms in anode are reduced into metal ions and enter electrolyte to replenish the loss from oxidation. The process is self sustaining until the metal atoms accumulate all the way to anode. This forms a conduction link between two electrodes; therefore, PMC reaches a low resistivity state that corresponds to logic '1'.

A reverse voltage bias will just do the opposite. This time cathode becomes source of reduction. The previous accumulated metal atoms on cathode will be reduced into ions and move toward anode. However, this process cannot sustain since once all metal atoms on cathode are oxidized, there is no longer any oxidation source, and the process will stop automatically. This reverse process dissolves the conduction link between electrodes; therefore, PMC cell returns to high resistivity state, which corresponds to logic '0'.

4.2 Device structure

Fig. 7 illustrates the structure of a PMC cell using silver based solid state electrolyte, as we reported in [26] and [27]. The device is fabricated on a glass substrate using aluminum cathode. We found that the thickness of solid state electrolyte layer has great effects on device performance. We will discuss the thickness dependence in detail in section 4.4. All three layers are evaporated using a thermal vacuum evaporator. In order to avoid spitting during evaporation, a special evaporation boat was designed for chalcogenide layer. The active layer thickness ranges from 8nm to 30nm.

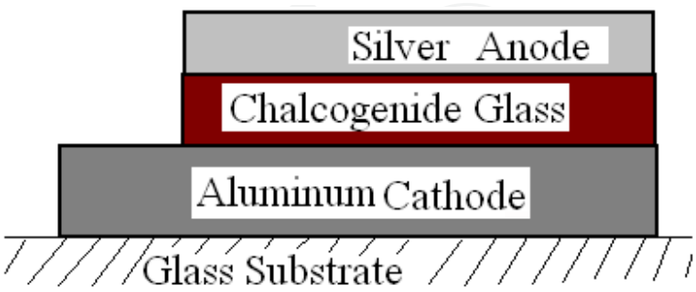


Fig. 7. Cross-section view of a PMC cell structure fabricated on glass substrate. This device is a silver-based PMC. [26]

4.3 Reading and writing process

Fig. 8 shows I-V characteristic of the above mentioned PMC cell. The active layer thickness of the testing device is 15nm. Electric current through PMC cell is measured using a

Keitheley source meter while voltage across device is tuned. Starting from 0V, voltage was increased up to 1V, then decreased to -1V, and finally brought back to 0V. We can clearly observe that the resistance of PMC device switches from high to low at 0.8V (SET voltage); and resistance switches from low to high at around -0.5V (RESET voltage). The measured 'ON" resistance (corresponds to logic '1') is 3 order of magnitude higher than the measured "OFF" resistance (corresponds to logic '0').

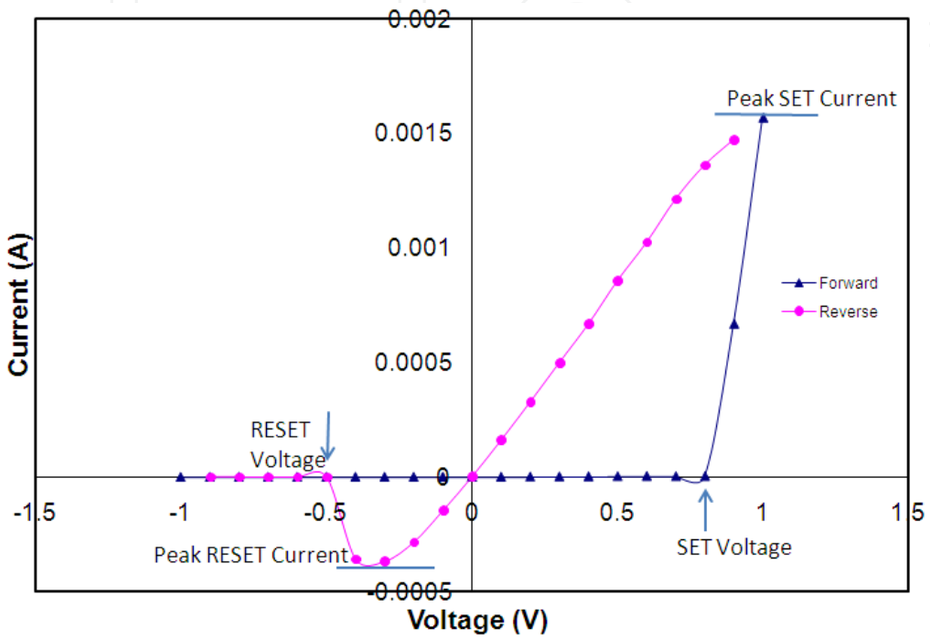


Fig. 8. I-V characteristic of a PMC testing cell. This cell is 100 by 100 μm and 60 nm in thickness. [8]

Therefore, the reading and writing process can be summarized as following:

1. SET

To SET PMC cell, a positive voltage pulse is needed. Since the electro-chemical process only need several ns to complete, a 30-50 ns SET pulse is enough. This, compared to SET pulse of PCM cell, is a significant advantage in term of device speed.

2. RESET

A negative voltage pulse is needed for RESET. This requires the access circuit of PMC cell allows access in both polarities. Therefore, a single access transistor is no longer enough. A possible access structure could be a NMOS transistor plus a PMOS transistor. This somewhat increased the complexity of memory circuit. However, since thermal isolation is not so essential for PMC memory as that for PCM memory, chip spaces for thermal isolation can be saved significantly. Therefore, PMC cell is still a highly scalable solution.

3. READ

A very low voltage pulse, as low as 0.1V, is needed for Reading. Similar to PCM reading, the device current is compared to a reference value. If device current is higher than reference, a logic '1' is identified; if device current is lower than reference, a logic '0' is identified. The typical resistance difference between logic '1' and '0' is at least 2 order of magnitude for PMC cell.

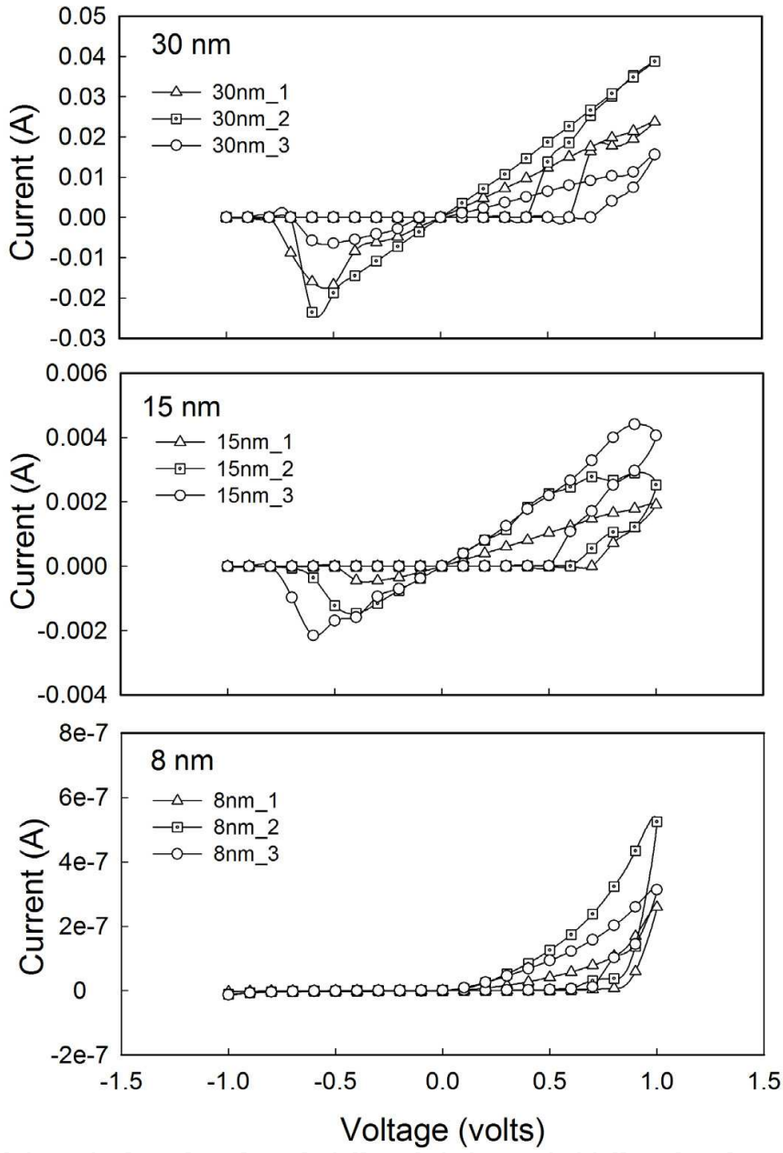


Fig. 9. I-V characteristic of PMC devices with different active layer thickness. Three devices are displayed for each thickness group. [27]

4.4 Effects of active layer thickness

Recently, Wang et. al studied the thickness dependency of PMC devices [27]. They found that the device metrics, such as R_{on}, R_{off} as well as switching threshold, has significant dependency on the active layer thickness. Fig. 9 shows the I-V characteristics of devices with thickness of 8nm, 15nm and 30nm. Table 1 summarizes the essential devices metrics for each thickness group.

From Table 1, one should notice that the devices with 8nm active layer thickness are not effectively conductive. This can be observed from Peak SET Current and Peak RESET Current. The Peak SET Current is less than a micro-ampere, while the Peak RESET Current is in nano-ampere range. The extremely small current is comparable to the parasitic current

in reading/writing control circuit, which brings difficulty to reading process. 15nm and 30nm devices do not have this problem.

Device Active Layer Thickness	8 nm (STD)	15nm (STD)	30nm (STD)
Peak SET Current (mA)	4.51E-04 (0.82E-04)	2.356 (1.04)	33.8 (7.92)
Peak RESET Current (mA)	-9.28E-06 (0.10E-06)	-1.123 (0.66)	-17.900 (4.23)
Average R_{off} (MΩ)	30.77 (7.78)	40.88 (9.91)	52.26 (11.12)
Average R_{on} (MΩ)	4.65 (0.69)	0.48 (0.14)	0.003 (0.0009)
Average R_{off}/R_{on}	5.05	137.6	18899.3
SET Voltage (V)	0.71 (0.025)	0.64 (0.054)	0.62 (0.13)
RESET Voltage(V)	0.05 (0.024)	0.46 (0.089)	0.57 (0.025)

Table 1. Average Device Parameters of three batches. Standard deviations are shown in parenthesis. [27]

The Peak SET Current and Peak RESET Current are both increasing as a function of active layer thickness. This is due to the reduced ON resistance (R_{on}) for thicker devices. The formation of conduction links during 'SET' process is an electrochemical deposition process, which always happens at surface first (in this case, electrolyte/cathode surface) [14]. This process relies on the availability of deposition nuclei and the prompt movement of Ag+ ions towards the surface. Therefore, the number of conduction links that can be formed mostly depends on the number of nuclei that can be formed at the beginning of this electrochemical deposition process. According to our previous work on Ag-Ge-S [15], the distribution of Ag+ in Ag-Ge-S electrolyte is not uniform. Rather, Ag+ ions are accumulated in some silver rich islands that are distributed in the backbone. Therefore, at the very beginning, Ag+ ions from islands near the surface tend to form nuclei. Once nuclei are formed, new comers of Ag+ ions would prefer to accumulate around the nuclei. For thinner electrolyte films, the distribution of Ag+ rich islands is dispersed and the size of those islands reduces too. Therefore, for 8nm devices, the formation of deposition nuclei is highly dispersed and not continuous. The result of this discontinuity is that less conduction links can be formed to connect cathode and anode. Moreover, when the active layer is thin, Ag's accumulation at cathodes localizes the Ag ions' movements due to the size of Ag (around 0.32nm in diameter). The overall effect is higher R_{on} for thinner devices.

It is also observed that the R_{off} of all 3 groups are roughly in the same order of magnitude, but slightly increase as a function of thickness. This is obvious since the resistance increases if one extends the length of the resistor. Therefore, the extremely large R_{off}/R_{on} ratio for 30nm devices is majorly due to their low ON resistance.

The SET voltage of the three groups shows very slightly decreasing trend as a function of thickness. This is probably due to the localization of Ag ions' movement in thinner devices. However, since the Ag ions move super fast, the difference among SET voltage is not very significant.

On the other hand, the RESET voltage shows significant discrepancy among three thickness groups. Overall, an increasing trend in RESET voltage is observed as a function of active layer thickness. While the RESET voltage is comparable between 15nm (0.64V) and 30nm (0.62V) devices, the RESET voltage of 8nm devices is significantly lower (0.05V) than that of

15nm and 30nm devices. Our explanation to this phenomenon is thicker devices (i.e. 30nm) have more conduction links once SET; hence, during RESET, more Ag atoms need to be ionized. This requires certainly higher reverse voltage. The 8nm group needs only -0.05 volt to RESET. Also notice, the R_{off}/R_{on} ratio of 8nm devices is only 5.05, significantly lower than that of 15nm and 30nm devices. This indicates that there were very few Ag conduction links formed in 8nm devices during 'SET' process due to dispersed deposition nuclei. Therefore, during RESET, there are not many Ag atoms on cathode to be ionized, which explains the low RESET voltage.

4.4 Current developments in the field

The first generation of programmable metallization cell was built based on metal containing chalcogenide solid electrolytes, such as Ag-Ge-S, Ag-Ge-S and Cu-Ge-S etc, with Ag or Cu as reactive electrodes. People then discovered that using Cu doped SiO_2 as the active medium of PMC is also viable. This new type of device has the advantage of easier integration with the current CMOS technology, since Cu is currently used as the interconnect metal in integrated circuits, while SiO_2 is known as the insulating material. However, unlike chalcogenide based devices, Cu can hardly be photodiffused into SiO_2. Instead, thermal diffusion or ion implantation has to be used to introduce Cu into SiO_2 backbone. Several groups reported the feasibility of fabricating Cu/SiO_2 based devices [34-35].

Approaches aiming to increase the data storage density is also vastly investigated for PMC devices. The research is diverted into two directions; one aims to improve the architecture of the device, i.e. 3-D devices [36] ; the other focuses on multilevel programming of the cell itself [37]. Russo et. al. [37] reported the knetics of the conductive filament's formation and growth during the programming can be controled by limiting the current compliance. The resistance of the cell can be tuned to 4 distinguished resistance states. This suggests the posibility of 2 bits storage of a single PMC cell.

5. Conclusion

In this chapter, we reviewed two non-volatile memory solutions based on chalcogenide glasses. PCM device is a relative mature solution now. PMC is a new concept and still in experimental stage. Non-volatile memory devices based on chalcogenide materials are the most promising replacement of charge-storage based memories due to its fast reading/writing speed and high scalability. In addition to those, since the information storage for chalcogenide devices are based on phase conversion or electrochemical reaction, chalcogenide based devices display excellent data retention characteristic when compared with charge-storage based devices.

6. Acknowledgment

Special thanks go to Dr. Punit Boolchand from University of Cincinnati for helps in bulk sample synthesis; Dr. Jagadeesh Moodera from MIT for helps in fabricating the masks; Dr. Richard Savage from California Polytechnic State University for helps in evaporator and characterization instruments.

7. References

[1] G S. R. Ovshingsky, "Reversible Electrical Switching Phenomena in Disordered Structures" *Phys. Rev. Lett.* 21 (1968) pp1450

[2] T. Ohta, "Phase-change optical memory promotes the DVD optical disk" *J. Optoelectron. Adv. Mater.* 3 (2001) pp609

[3] J. Siegel, A. Schropp, J. Solis, C.N. Afonso, M.Wuttig, "Rewritable phase-change optical recording in $Ge_2Sb_2Te_5$ films induced by picosecond laser pulses" *Appl. Phys. Lett.* 84 (2004) 2250

[4] T. Ohta, E.R. Ovshynsky, in *Photo-Induced Metastavility in Amorphous Semiconductors*, edited by A.V. Kovobov, Wiley-VCH, Weinheim, (2003) p. 310

[5] M.N. Kozicki, M. Yun, S. J. Yang, J.P Aberouette, J.P. Bird, "Nanoscale effects in devices based on chalcogenide solid solutions" *Superlattices and Microstructures,* 27 (2000) No. 5/6, pp485-488

[6] M. N. Kozicki, C. Gopalan, M. Balakrishnan, M. Park, M. Mitkova, "Nonvolatile memory based on solid electrolytes" *Non-Volatile Memory Technology Symposium Proceedings* (2004) 15-17

[7] I. Chaitanya et al. "Metal-semiconductor-metal Junctions with silver sulfide barrier layer" presentation at *American Physical Society March Meeting, Baltimore, MD*, (2006) (unpublished)

[8] Carter De Leo, Senior Project Report, California Polytechnic State University (2007)

[9] Sakamoto et al. "Nanometer-scale switches using copper sulfide" *Appl. Phys. Lett.* 82 (2003) pp3032

[10] S.Chakravarty, D.G.Georgiev, P.Boolchand and M.Micoulaut, "Ageing, fragility and the reversibility window in bulk alloy glasses", *J. Phys. Condens*. Matter, 17, (2005) L1-L7

[11] D.G.Georgiev, P.Boolchand and M.Micoulaut , "Rigidity transitions and molecular structure of As_xSe_{1-x} glasses." *Phys.Rev. B* 62, 14 (2000) pp9268

[12] Tao Qu, D.G. Georgiev, P.Boolchand and M.Micoulaut, "The Intermediate Phase in Ternary GexAsxSe1-2x Glasses" *Mat. Res. Soc. Symp. Proc.* 754 (2003) pp111

[13] Tao Qu and P.Boolchand, "Shift in elastic phase boundaries due to nanoscale phase separation in network glasses: the case of $Ge_xAs_xS_{1-2x}$". *Phil. Mag,* 85, (2005), pp875

[14] D. Selvanathan, W.J.Bresser and P. Boolchand, "Stiffness transitions in Si_xSe_{1-x} glasses from Raman scattering and temperature-modulated differential scanning calorimetry." *Phys. Rev B* 61, (2000) pp15061

[15] P.Boolchand, D.G.Georgiev and B. Goodman , "Discovery of the intermediate phase in chalcogenide glasses" *J.Opto. and Adv. Mater. 3* (2001) pp703.

[16] J.C. Phillips, "Universal Intermediate Phases of Dilute Electronic and Molecular Glasses" *Phys. Rev. Lett.* 88, (2002) 216401

[17] M.F. Thorpe, D.J. Jacobs, M.V. Chubynsky, and J.C.Phillips, "Self-organization in network glasses" *J. Non-Cryst. Solids* 266-269 (2001) pp859

[18] M.Micoulaut and J.C.Phillips, "Rings and rigidity transitions in network glasses" *Phys. Rev. B 67* (2003) 104204.

[19] P.Boolchand, X.Feng, W.J.Bresser, "Rigidity transition in binary Ge-Se glasses and intermediate phase" *J. Non- Cryst. Solids* 293-295 (2001) pp348

[20] X. Feng, W.J. Bresser, P.Boolchand, "Direct Evidence for Stiffness Threshold in Chalcogenide Glasses" *Phys. Rev. Lett.* 78 (1997) pp4422

[21] Fei Wang, S. Mamedov, P. Boochand and B. Goodman, "Pressure Raman effects and internal stress in network glasses" *Physical Rev B*. 71 (2005) pp174210

[22] Fei Wang, P. Boolchand and K. A. Jackson, "Chemical Alloying and light-induced collapse of the intermediate phase in chalcohalide glasses" *J. Phys.: Condens. Matter* 19 (2007) pp226201

[23] Woo Yeong Cho et al. "A 0.18-/spl mu/m 3.0-V 64-Mb nonvolatile phase-transition random access memory (PRAM)" *IEEE Journal of Solid State Circuits*, Vol 40, No. 1 (2005) pp293-300

[24] Byung-Do Yang, Jae-Eun Lee, Jang-Su Kim and Junghyun Cho, "A Low Power Phase-change Random Access Memory using a Data-Comparison Write Scheme" *Proceeding of IEEE International Symposium on Circuit and Systems*, (2007) pp3014-3017

[25] A. Antonaia, M.C. Santoro, G. Fameli and T. Polichetti, "Transport mechanism and IR structural characterisation of evaporated amorphous WO_3 films" *Thin Solid Films*, Vol 426 (2003) pp281-287

[26] P.W. Dunn, Master Thesis, California Polytechnic State University, (2008) (unpublished)

[27] F. Wang, P.W. Dunn, M. Jain, C. De Leo and N. Vickers, "The effects of active layer thickness on programmable metallization cell based on Ag-Ge-S", Solid State Electronics, in press (2011)

[28] S. Song, Z. Song, Y. Lu, B. Liu, L. Wu and S. Feng,"Sb2Te3-Ta2O5 nano-composite films for low-power phase-change memory application", Materials Letters 64 (2010) pp2718-2730

[29] H.Y. Cheng, K.F. Kao, C.M. Lee and T.S. Chin,"Crystallization kinetics of Ga–Sb–Te films for phase change memory „ Thin Solid Films 516 (2008) pp5513-5517.

[30] T.C. Chong, L.P. Shi, R. Zhao, P.K. Tan, J.M. Li, K.G. Lim and L.P. Shi," Phase change random access memory cell with superlattice-like structure„ Applied Physical Letters 88 (2006) pp122144.

[31] C. Wang, S. Li, J. Zhai, B. Shen, M. Sun and T. Lai,"Rapid crystallization of SiO2/Sb80Te20 nanocomposite multilayer films fro phase-change memory applications" Scripta Materialia 64 (2011) pp 645-648

[32] Y. Gu, Z. Song, T. Zhang, B. Liu and S. Feng,"Novel phase-change material GeSbTe for application of three-level phase-change random access memory", Solid State Electronis 54 (2010) pp443-446

[33] Y. Yin and S. Hosaka,"Multilevel storage in lateral phase-change memory by promotion of nanocrystallization", Microelectronic Engineering, in press (2011)

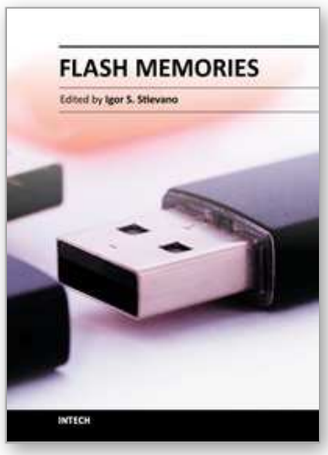
[34] S. Puthen Thermandam, S.K. Bhagat, T.L. Alford, Y. Sakaguchi, M.N. Kozicki and M. Mitkova,"Influence of Cu diffusion conditions on the switching of Cu-SiO_2-based resistive memory devices", Thin Solid Films, 518 (2010), pp3293-3298

[35] Y. Bernard, V.T. Renard, P. Gonon and V. Jousseaume,"Back-end-of-line compatible Conductive Bridging RAM based on Cu and SiO_2", Microelectronic Engineering (2010) in press

[36]C. Kugeler, M. Meier, R. Rosezin, S. Gilles and R. Waser,"High density 3D memory architecture based on the resistive switching effect", Solid State Electronics 53 (2009) pp1287-1292

[37] U. Russo, D Kamalanathan, D. Ielmini, A. Lacaita and M. Kozicki,"Study of multilevel programming in programmable metallization cell memory", IEEE Transaction on Electron Devices, 56, No. 5 (2009) pp1040-1047

[38] R. Bez and A. Pirovano,"Non-volatile Memory technologies: emerging concepts and new materials" , Material Science in Semiconductor Processing, vol. 7 (2004) pp349-355



Flash Memories

Edited by Prof. Igor Stievano

ISBN 978-953-307-272-2

Hard cover, 262 pages

Publisher InTech

Published online 06, September, 2011

Published in print edition September, 2011

Flash memories and memory systems are key resources for the development of electronic products implementing converging technologies or exploiting solid-state memory disks. This book illustrates state-of-the-art technologies and research studies on Flash memories. Topics in modeling, design, programming, and materials for memories are covered along with real application examples.

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

Fei Wang (2011). Non-Volatile Memory Devices Based on Chalcogenide Materials, Flash Memories, Prof. Igor Stievano (Ed.), ISBN: 978-953-307-272-2, InTech, Available from: http://www.intechopen.com/books/flash-memories/non-volatile-memory-devices-based-on-chalcogenide-materials

INTECH
open science | open minds

InTech Europe
University Campus STeP Ri
Slavka Krautzeka 83/A
51000 Rijeka, Croatia
Phone: +385 (51) 770 447
Fax: +385 (51) 686 166
www.intechopen.com

InTech China
Unit 405, Office Block, Hotel Equatorial Shanghai
No.65, Yan An Road (West), Shanghai, 200040, China
中国上海市延安西路65号上海国际贵都大饭店办公楼405单元
Phone: +86-21-62489820
Fax: +86-21-62489821

IntechOpen