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Numerical Simulation of Transient Response in 3-D Multi-Channel Nanowire MOSFETs Submitted to Heavy Ion Irradiation

Daniela Munteanu, Jean-Luc Autran and Sébastien Martinie
*IM2NP Laboratory, CNRS (Centre National de la Recherche Scientifique),
Aix-Marseille University
France*

1. Introduction

The bulk MOSFET scaling has recently encountered significant limitations, mainly related to the gate oxide (SiO_2) leakage currents (Gusev et al., 2006; Taur et al., 1997), the large increase of parasitic short channel effects and the dramatic mobility reduction (Fischetti & Laux, 2001) due to highly doped Silicon substrates precisely used to reduce these short channel effects. Technological solutions have been proposed in order to continue to use the “bulk solution” until the 32 nm ITRS node (ITRS, 2009). Most of these solutions envisage the introduction of high-permittivity gate dielectric stacks (to reduce the gate leakage, (Gusev et al., 2006; Houssa, 2004), midgap metal gate (to suppress the Silicon gate polydepletion-induced parasitic capacitances) and strained Silicon channel (to increase carrier mobility (Rim et al., 1998). However, in parallel to these efforts, alternative solutions to replace the conventional bulk MOSFET architecture have been proposed and studied in the recent literature. One solution is the radical change of the device architecture such as in Multiple-Gate devices introducing additional gate electrodes: 2 (double-gate), 3 (FinFET or trigate) or 4 (gate-all-around, completely surrounding the channel). Silicon nanowires MOSFETs with gate-all-around (GAA) provide an original and very promising architecture to further increase the integration density and performances of nano-devices (Park & Colinge, 2002). These structures exhibit a superior control of short channel effects resulting from an exceptional electrostatic coupling between the conduction channel and the surrounding gate electrode. As a result, intrinsic channels can be used leading to higher mobilities and drain currents.

3D Multi-Channel MOSFETs (MCFETs) have been recently proposed to achieve a higher current drivability and a significant enhancement of the on-state current over the off-state current ratio ($I_{\text{ON}}/I_{\text{OFF}}$) (Bernard et al., 2007; Ernst et al., 2006) compared to conventional single channel devices. MCFETs combine the advantages of excellent control of short-channel effects with a high on-state current due to a multiple-gate architecture and the 3-D integration of vertically stacked channels. GAA devices with ultra-thin and narrow channels (about 10 nm) are seen as the ideal architecture for off-state current control of sub-10 nm gate lengths (Ernst et al., 2006). Meanwhile, the current density per surface of such a device is limited by the lithography pitch, which dictates the distance between nanowires. The

current density can be improved by the vertical integration of GAA devices. Thanks to vertical stacked channels, a 5× increase in current density per layout surface can be achieved compared to planar transistors with the same gate stack (Ernst et al., 2006).

As the MOSFET is scaling down, the sensitivity of integrated circuits to radiation, coming from the natural space or present in the terrestrial environment, has been found to seriously increase (Baumann, 2005; Dodd, 1996; Dodd & Massengill, 2003; Dodd, 2005). In particular, ultra-scaled memory ICs are more sensitive to single-event-upset (SEU) and digital devices are more subjected to digital single-event transient (DSETs). Single-event-effects (SEE) are the result of the interaction of highly energetic particles, such as protons, alpha particles, or heavy ions, with sensitive regions of a microelectronic device or circuit. These SEE may perturb the device/circuit operation (e.g., reverse or flip the data state of a memory cell, latch, flip-flop, etc.) or definitively damage the circuit (e.g. gate oxide rupture, destructive latch-up events).

The physical mechanisms related to the production of SEE in microelectronic devices consist in three main successive steps: (1) the charge deposition by the energetic particle striking the sensitive region, (2) the transport of the released charge into the device and (3) the charge collection in the sensitive region of the device. In the following we succinctly describe these different mechanisms, for a detailed presentation we invite the reader to consult (Baumann, 2005; Dodd, 1996; Dodd & Massengill, 2003; Dodd, 2005).

Charge deposition (or generation): When an energetic particle strikes the device, an electrical charge can be deposited by one of the following mechanisms: direct ionization by the interaction with the material or indirect ionization, by secondary particles issued from nuclear reactions with the atoms of the struck material. Direct ionization typically characterizes heavy ions ($Z \geq 2$) of the space environment. They interact with the target material mainly by inelastic interactions and transmit a large amount of energy to the electrons of the struck atoms. These electrons produce a cascade of secondary electrons which thermalize and create electron-hole pairs along the particle path. In a semiconductor or insulator, a large amount of the deposited energy is thus converted into electron-hole pairs, the remaining energy being converted into heat and a very small quantity in atoms displacement. It was experimentally shown that the energy necessary for the creation of an electron-hole pair depends on the material bandgap. In a Silicon substrate, one electron-hole pair is produced for every 3.6 eV of energy lost by the ion. Other particles, such as neutrons of the terrestrial environment, do not interact directly with target material since they do not ionize the matter on their passage. However, these particles should not be neglected, because they can produce SEE due to their probability of nuclear reaction with the atoms of materials which compose the microelectronic devices. This mechanism is called indirect ionization. The products resulting from a nuclear reaction can deposit energy along their traces, in the same manner as that of direct ionization. Since the creation of the column of electron-hole pairs of these secondary particles is similar to that of ions, the same models and concepts can be used.

Charge transport: When a charge column is created in the semiconductor by an ionizing particle, the released carriers are quickly transported and collected by elementary structures (e.g. p-n junctions). The transport of charge relies on two main mechanisms: the charge drift in regions with an electric field and the charge diffusion in neutral zones. The deposited charges can also recombine with other mobile carriers existing in the crystal lattice.

Charge collection: The charges transported in the device induce a parasitic current transient, which could induce disturbances in the device and associated circuits. The devices most sensitive to ionizing particle strikes generally contain reversely-biased p-n junctions, because the strong electric field existing in the depletion region of the p-n junction allows a very efficient collection of the deposited charge. The effects of ionizing radiation are different according to the intensity of the current transient, as well as the number of impacted circuit nodes. If the current is sufficiently important, it can induce a permanent damage on gate insulators (gate rupture, SEGR) or the latch-up (SEL) of the device. In usual low power circuits, the transient current may generally induce only an eventual change of the logical state (cell upset).

Modeling and simulating the effects of ionizing radiation has long been used for better understanding the radiation effects on the operation of devices and circuits. In the last two decades, due to substantial progress in simulation codes and computer performances which reduce computation times, simulation reached an increased interest. Due to its predictive capability, simulation offers the possibility to reduce radiation experiments and to test hypothetical devices or conditions, which are not feasible (or not easily measurable) by experiments. Physically-based numerical simulation at device-level presently becomes an indispensable tool for the analysis of new phenomena specific to short-channel devices (non-stationary effects, quantum confinement, quantum transport), and for the study of radiation effects in new device architectures (such as multiple-gate, Silicon nanowire MOSFET), for which experimental investigation is still limited. In these cases, numerical simulation is an ideal investigation tool for providing physical insights and predicting the operation of future devices expected for the end of the roadmap. A complete description of the modeling and simulation of SEE, including the history and the evolution of this research domain, have been presented in the survey papers by Dodd (Dodd, 1996; Dodd & Massengill, 2003; Dodd, 2005) and Baumann (Baumann, 2005). It is also important to note that phenomena related to an ionizing particle striking a microelectronic device are naturally three dimensional (3-D) mechanisms, due to both the tri-dimensional structure of the ion track and the 3-D structure of real devices. 3-D simulation is then necessary not only for actual short/narrow devices, but also for new device architectures for which 3-D electrostatic or quantum confinement effects cannot be taken into account in a 2-D simulation. 3-D simulation is also necessary when considering non-normal incidence of the ion strike on the device.

In this chapter, we investigate the transient response of MCFETs submitted to heavy ion irradiation using 3-D numerical simulation. The MCFET contains GAA and FinFET nanowire MOSFETs with ultra-thin, narrow channels (10 nm) and a 32 nm channel length. Recent simulation studies have shown that GAA MOSFET devices are less sensitive to single event transients (SET) than fully-depleted single-gate SOI devices (Francis et al., 1995; Munteanu et al., 2006; Munteanu et al., 2007). This is due to the improved control of the channel potential which reduces floating body effects and improves the device immunity to single event transients. MCFET devices are then expected to show a very low sensitivity to ionizing radiation.

This chapter is organized as follows: after the presentation of the 3-D simulated structures and simulation models (sections II and III), we will analyze in section IV the effect of the ion strike on the main internal electrical parameters inside the structure and on the drain current transient. In this section we will compare the sensitivity to heavy ion irradiation of

the MCFETs with that of other single and multiple-gate devices. Finally, in section V we will investigate the influence of the ion strike parameters (location, direction, and radius of the ion track) and of the lateral spacing between the nanowire stacks on the current transient and charge collection.

2. Description of simulated devices

The structure of the simulated MCFETs is a 3×3 nanowire matrix containing square cross-section nanowires. The description of the 3-D architecture considered here and the definition of the geometrical parameters are shown in Fig. 1. The MCFET matrix is composed of three parallel transistor stacks, each stack containing 3 vertically stacked nanowire devices (2 GAA and 1 FinFET). The MCFET is calibrated to fill the ITRS'2009 (ITRS, 2009) low-power (LP) requirements in terms of off-state current for the technology nodes corresponding to the year 2009 ($I_{\text{OFF}} < 5 \times 10^{-3} \text{ A}/\mu\text{m}$). The individual nanowire MOSFETs are designed with a 32 nm gate length, square cross-section with $t_{\text{Si}}=W=10 \text{ nm}$, and a 3 nm-thick gate oxide. An intrinsic silicon film and a midgap gate are considered. Three lateral spacings, s , between the nanowire stacks are considered: 100, 75, and 50 nm.

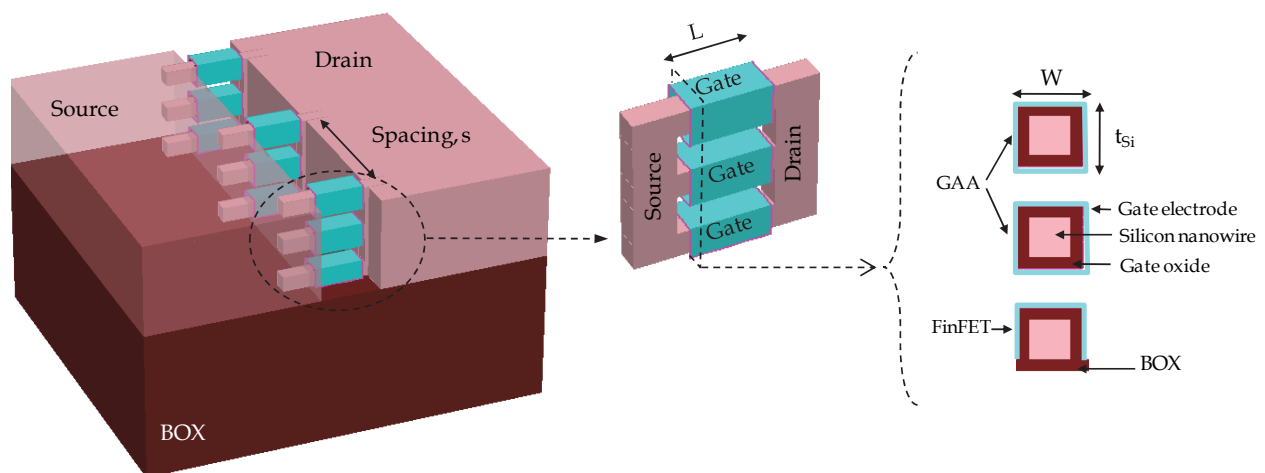


Fig. 1. Schematic description of the 3-D simulated MCFET structures and their main geometrical parameters. The MCFET matrix is composed of three parallel transistor stacks, each stack containing 3 vertically stacked nanowire devices (2 GAA and 1 FinFET). All nanowires have silicon film with square section ($t_{\text{Si}}=W=10 \text{ nm}$). For a better view of the nanowires the gate material, spacers, isolation oxide and a part of the source and drain regions are not shown.

3. Description of the simulation approach

3-D numerical simulations have been performed with the DESSIS device simulator from the 3-D Sentaurus code (Sentaurus, 2009). The main models used in simulation are the doping-dependent Shockley-Read-Hall and Auger recombination models and the Fermi-Dirac carrier statistics. The model of the effective intrinsic density includes doping-dependent band-gap narrowing (Slotboom model (Sentaurus, 2009)) and a lattice temperature-dependent band gap. The hydrodynamic model was used for the carrier transport equations, including the energy balance equations for electrons, holes, and the lattice. The

impact ionization and the carrier mobility models depend on carrier energy calculated with the hydrodynamic model. The mobility model includes dependencies on the lattice temperature, channel doping level and normal electric field through the Lombardi model (Sentaurus, 2009). In the following we succinctly describe the hydrodynamic transport model used in the present simulation approach.

3.1 Transport model

Historically, the first models used in carrier transport simulation described the physical phenomena taking place in the device as functions of the electric field, even if these phenomena depend on carrier energy (Selberrer, 1984). This is possible when considering that carrier energy is in permanent balance with the electric field. Carrier transport in MOSFET devices is mainly due to electrostatic potential gradients and/or gradients of carrier concentration (Selberrer, 1984). The current density in a biased device is then usually modeled by the sum of a conduction component (drift) and a diffusion component, as follows (for electrons):

$$J_n = q\mu_n nE + qD_n \nabla n \quad (1)$$

where q is the elementary charge, μ_n is the carrier mobility, D_n is the thermal diffusion coefficient, E is the electric field and n is the electron density. D_n and μ_n depend on material and electric field and are connected by the Einstein's equation:

$$D_n = \mu_n \frac{kT_L}{q} \quad (2)$$

with T_L the lattice temperature and k is the Boltzmann constant. Similar equations are considered for holes (see the paragraph "Drift-Diffusion" below).

This traditional description of electronic transport constitutes the "Drift Diffusion" (DD) model, the basic model used in CMOS devices simulation (Lundstrom, 2000; Selberrer, 1984). This modeling level is generally adapted for long devices, with either weak or strong electric fields (except for the modeling of impact ionization; see below in this paragraph). When the device feature size is reduced, the electronic transport becomes qualitatively different from the traditional transport model since the average carrier velocity does not depend on the local electric field. Average carrier velocity is a function of the carrier energy which depends on the variations in time and space of the electric field. In short devices, steep variations of electric field take place in the active area of the devices. Then, non-stationary phenomena (such as velocity overshoot (Baccarani & Wordeman, 1985; Jacoboni & Reggiani, 1983) occur following these rapid spatial or temporal changes of high electric fields. In small devices, non-stationary phenomena play an important role and may dominate the device operation. Since DD model neglects non-stationary effects, new advanced transport models become mandatory for accurate transport simulation in ultra-short devices (Apanovich et al., 1994; Blotekjaer, 1970; Stratton, 1962).

The DD model considers that carriers gain maximum energy instantaneously balanced with the electric field (Lundstrom, 2000). Consequently, non-stationary effects (velocity overshoot and carrier transport by thermal diffusion processes associated with electronic temperature gradients) specific to short devices are neglected in DD model, as well as the dependence of impact ionization on the carrier energy.

In reality, the carrier energy does not immediately respond to changes in electric field. Mobility and diffusion coefficients are tensor quantities that depend on several parameters besides electric field (Khanna, 2004). In ultra-short MOSFETs (deca-nanometre channel lengths), the high internal electric fields result in substantial electron heating. The hydrodynamic model, obtained by taking the first three moments of the Boltzmann Transport Equation (BTE), represents the carrier transport effects in short devices more accurately than the DD model. The hydrodynamic model is a macroscopic approximation to the BTE taking into account the relaxation effects of energy and momentum. In this model, the propagation of electrons in a semiconductor is treated as the flow of a charged, thermally conducting gas subjected to an electric field. This model removes several limiting assumptions of DD: the carrier energy can exceed the thermal energy and all physical parameters are energy-dependent. The current density and the energy flow are modelled in HD model by the following equations (given here for electrons (Sentaurus, 2009)):

$$\vec{J}_n = q\mu_n \left[-n\vec{\nabla}\phi + \frac{kT_n}{q}\vec{\nabla}n + \frac{k}{q}(1 + \xi_n)n\vec{\nabla}T_n \right] \quad (3)$$

$$\text{div}\vec{S}_n = -\vec{J}_n\vec{\nabla}\phi - \frac{3k}{2}\frac{\partial}{\partial t}(nT_n) - W_n \quad (4)$$

$$\vec{S}_n = -K_n\vec{\nabla}T_n - \frac{k\Delta_n}{q}\vec{J}_nT_n \quad (5)$$

where T_n is the electron temperature, ξ_n is a model coefficient, \vec{S}_n is the energy flow, W_n is the energy density loss rate, K_n is the thermal conductivity and:

$$\Delta_n = \frac{5}{2} + \xi_n \quad (6)$$

while the energy density loss W_n is given by:

$$W_n = \frac{3}{2}n\frac{k(T_n - T_L)}{\tau_{rel}} + \frac{3}{2}kT_nR_{SRH} + E_g(G_n - R_n^A) \quad (7)$$

where τ_{rel} is the energy relaxation time, R_{SRH} is the SRH recombination rate, G_n is the impact ionization rate, R_n^A is the Auger recombination rate, E_g is the Silicon bandgap. Similar equations are used for holes. Usually, the mobility μ_n is modelled as a decreasing function of energy (because the scattering rate increases with the energy of the particle). Finally, the system of equations of the HD model is completed by the continuity equations:

$$\text{div}\vec{J}_n = qR + q\frac{\partial n}{\partial t} \quad (8)$$

$$\text{div}\vec{J}_p = -qR - q\frac{\partial p}{\partial t} \quad (9)$$

where R is the generation-recombination rate.

3.2 Modeling the effect of a particle strike

The radiation effects have been simulated using the HeavyIon module of the TCAD Sentaurus toolsuite (Sentaurus, 2009), considering an electron-hole pair column centred on the ion track axis to model the ion strike. The ion track structure to be used as input in simulation is presently a major issue for device simulation. The first representations included a simple cylindrical charge generation with a uniform charge distribution and a constant LET along the ion path. However, the real ion track structure is radial and varies as the particle passes through the matter. When the particle strikes a device, highly energetic primary electrons (called δ -rays) are released. They further generate a very large density of electron-hole pairs in a very short time and in a very small volume around the ion trajectory, referred as the ion track. These carriers are collected by both drift and diffusion mechanisms, and are also recombined by different mechanisms of direct recombination (radiative, Auger) in the very dense core track, which strongly reduces the peak carrier concentration. All these mechanisms modify the track distribution both in time and space. As the particle travel through the matter, it loses energy and then the δ -rays become less energetic and the electron-hole pairs are generated closer to the ion path. Then, the incident particle generates characteristic cone-shaped charge plasma in the device (Dodd, 2005).

The real ion track structure has been calculated using Monte-Carlo methods (Hamm et al., 1979; Martin et al., 1987; Oldiges et al., 2000). These simulations highlighted important differences between the track structure of low-energy and high-energy particles, even if the LET is the same (for details see (Dodd et al., 1998; Dodd, 2005)). High-energy particles are representative for ions existing in the real space environment, but they are not available in typical laboratory SEU measurements (Dodd, 1996). Then the investigation of the effects of high-energy particles by simulation represents an interesting opportunity, which may be difficult to achieve experimentally.

Analytical models for ion track structure have been also proposed in the literature and implemented in simulation codes. One of the most interesting models is the “non-uniform power law” track model, based on the Katz theory (Kobetich & Katz, 1968) and developed by Stapor (Stapor & McDonald, 1988). In this model, the ion track has a radial distribution of excess carriers expressed by a power law distribution and allows the charge density to vary along the track (Dussault et al., 1993). Other analytical models propose constant radius non-uniform track or Gaussian distribution non-uniform track.

In commercial simulation codes, the effect of a particle strike is taken into account as an external generation source of carriers. The electron-hole pair generation induced by the particle strike is included in the continuity equations via an additional generation rate. This radiation-induced generation rate can be connected to the parameters of irradiation, such as the particle Linear Energy Transfer (LET). The LET is the energy lost by unit of length ($-dE/dl$), which is expressed here in MeV cm²/mg (1pC/ μ m \approx 100 MeV cm²/mg). The particle LET can be converted into an equivalent number of electron-hole pairs by unit of length using the mean energy necessary to create an electron-hole pair (E_{ehp}) (Roche, 1999):

$$\frac{dN_{ehp}}{dl} = \frac{1}{E_{ehp}} \frac{dE}{dl} \quad (10)$$

where N_{ehp} is the number of electron-hole pairs created by the particle strike. By associating two functions describing the radial and temporal distributions of the created electron-hole pairs, the number of electron-hole pairs is included in the continuity equations (Munteanu & Autran, 2008) via the following radiation-induced generation rate:

$$G(w, l, t) = \frac{dN_{ehp}}{dl}(l) \cdot R(w) \cdot T(t) \quad (11)$$

where $R(w)$ and $T(t)$ are the functions of radial and temporal distributions of the radiation induced pairs, respectively. Equation (11) assumes the following hypothesis: the radial distribution function $R(w)$ depends only on the distance traversed by the particle in the material and the generation of pairs along the ion path follows the same temporal distribution function in any point. Since function G must fill the condition:

$$\int_{w=0}^{\infty} \int_{\theta=0}^{2\pi} \int_{t=-\infty}^{\infty} G w dw d\theta dt = \frac{dN_{ehp}}{dl} \quad (12)$$

functions $R(w)$ and $T(t)$ are submitted to the following normalization conditions:

$$2\pi \int_{w=0}^{\infty} R(w) w dw = 1 \quad (13)$$

$$\int_{t=-\infty}^{\infty} T(t) dt = 1 \quad (14)$$

The ion track models available in commercial simulation codes usually propose a Gaussian function for the temporal distribution function $T(t)$:

$$T(t) = \frac{e^{-\left(\frac{t}{t_c}\right)^2}}{t_c \sqrt{\pi}} \quad (15)$$

where t_c is the characteristic time of the Gaussian function which allows one to adjust the pulse duration. The radial distribution function is usually modelled by an exponential function or by a Gaussian function:

$$R(w) = \frac{e^{-\left(\frac{w}{r_c}\right)^2}}{\pi r_c^2} \quad (16)$$

where r_c is the characteristic radius of the Gaussian function used to adjust the ion track width. Previous works have demonstrated that the different charge generation distributions used for the radial ion track does affect the device transient response, but the variation is typically limited to ~5% for ion strikes on bulk p-n diodes (Dodd, 2005; Dussault et al., 1993). Considering a LET which is not constant with depth along the path has a more significant impact on the transient response in bulk devices. The key parameters of the single event transient (peak current, time to peak and collected charge) have up to 20% variation when LET is allowed to vary with depth compared to the case of a constant LET (Dussault et al., 1993). Nevertheless, the LET variation with depth has no influence on the transient response of actual SOI devices with thin Silicon film.

In the following simulations, two characteristic radii have been considered for the spatial Gaussian dependence of the ion track: 50 and 20 nm. The Gaussian time distribution (Eq. (15)) is centered on 10 ps and has a characteristic width of 2 ps. The linear energy transfer (LET)

value is kept constant along the track. The ion strikes the middle of the channel between the source and the drain and perpendicular to the gate electrode, as shown in Fig. 2. The different ion strike locations considered in this work are schematically presented in Fig. 2.

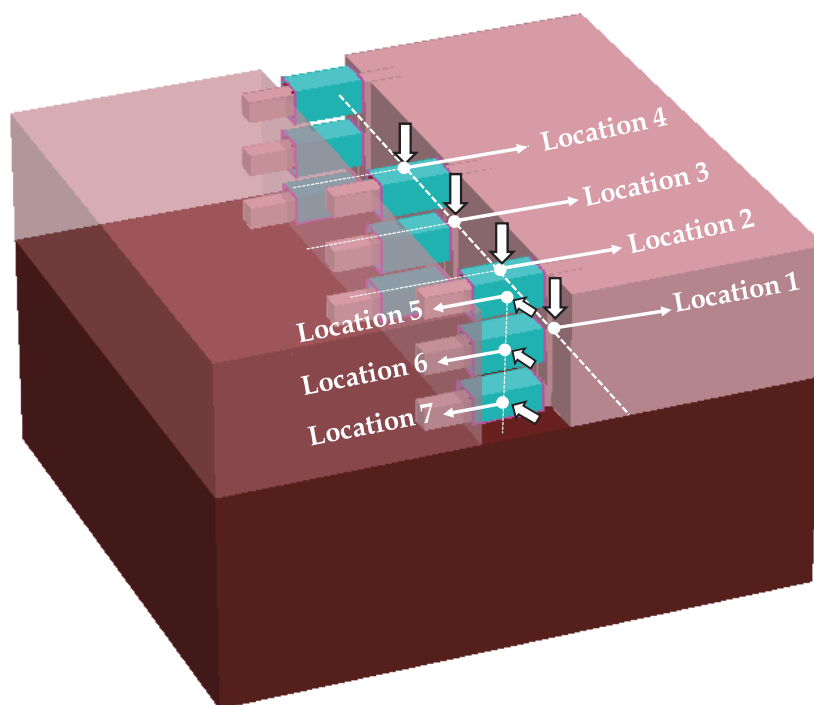


Fig. 2. Positions (arrows) of the ion strike considered in this work; the ion strikes in the middle of the channel (between the source and drain regions). For a better view of the nanowires, the gate material, spacers and isolation oxide are not shown.

Ion strike locations labelled "1", "2", "3", and "4" are parallel to the y-axis (perpendicular to the x-z plane) and the ion strike locations "5", "6", and "7" are parallel to the z-axis (perpendicular to the x-y plane). The lateral spacing between locations "1", "2", "3", and "4" are equal to $s/2$. The 3-D profile of heavy ion charge density generated in the structure is shown in Fig. 3 for the ion strike locations "1", "2", "3", and "4". The MCFET is biased in the off-state ($V_G=0$ V). The drain terminal is constantly biased at 0.8 V. The collected charge is derived by integrating the drain current over the transient duration.

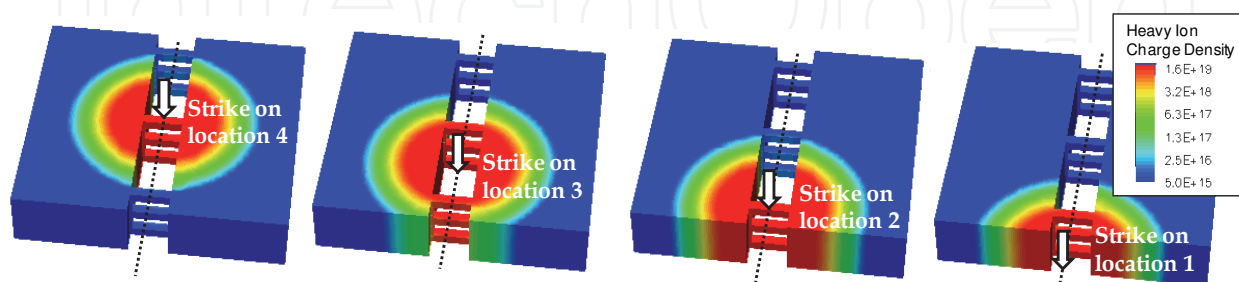


Fig. 3. 3-D profile of the heavy ion charge density for the ion strike locations "1", "2", "3", and "4". The positions (arrows) of the ion strike considered in this work are also shown; the ion strikes in the middle of the channel (between the source and drain regions). For a better view of the nanowires, the gate material, spacers and isolation oxide are not shown.

4. Transient simulation results

4.1 Potential and carrier density

Figure 4 shows the 3-D profiles of the electrostatic potential (Fig. 4(a)) and the electron density (Fig. 4(b)) in a 3-D MCFET with a lateral spacing $s=100$ nm for the ion strike location "2" at $t=10$ ps (maximum generated charge by the ion strike). The ion track radius considered here is equal to 50 nm. This figure shows that the electrostatic potential profile is perturbed by the ion strike, especially in the first nanowire stack that is struck directly. However, the impact is less visible in the second nanowire stack and is almost undetectable for the third nanowire stack (situated the farthest from the ion strike impact location). For a better view of the potential variation in the MCFET stacks, we plot in Fig. 5 the potential in a cutline along the x-axis in the middle of the channel at different times before and after the ion strike. Two devices are considered: the impacted transistor located in the first nanowire stack (Fig. 5(a)) and the nanowire symmetrically situated in the third nanowire stack (Fig. 5(b)). The variation with time of the potential in the impacted transistor indicates that the parasitic bipolar device is turning on. On the contrary, the potential in the third nanowire stack varies only very slightly, as shown in Fig. 5(b). This is due to the narrow ion track radius compared to the lateral spacing between nanowires.

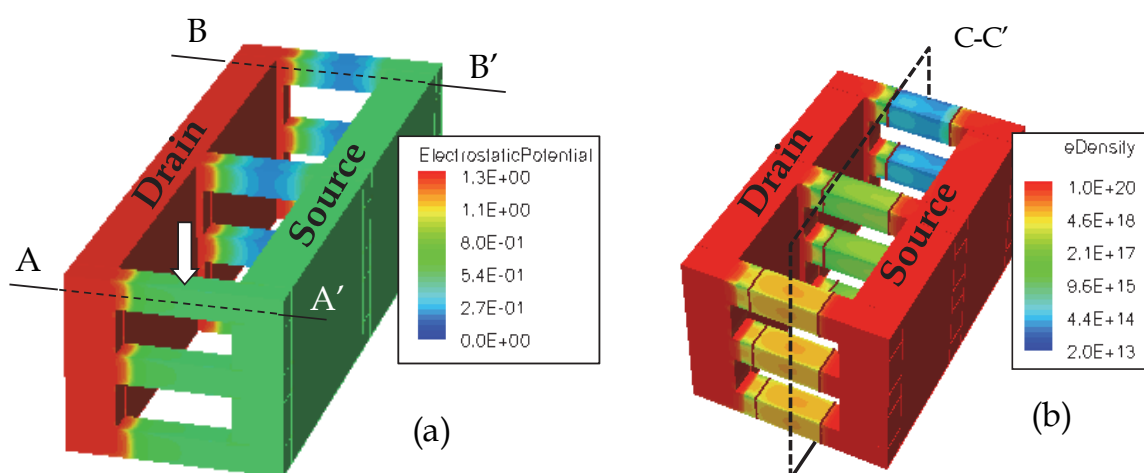


Fig. 4. 3-D profile of electrostatic potential (a) and of electron density (b) in the 3-D MCFET for the ion strike location "2" at $t=10$ ps. For a better view of the nanowires, the gate material, spacers, isolation oxide, and a part of the source and drain regions are not shown. The MCFET is biased in the off-state ($V_G=0$ V, $V_D=0.8$ V). The nanowire spacing is $s=100$ nm, the ion strike LET is 10 MeV/(mg/cm²), and the ion track radius is 50 nm. The ion strike location is indicated by the arrow.

The 2-D profiles of the electron density in a cross-section in the MCFET (cut plane C-C' indicated in Fig. 4(b)) are reported in Fig. 6 before and after the ion strike in location "2". These profiles give details concerning the distribution inside each nanowire. The electron density is centered in the middle of the film for the GAA devices, which is a typical feature of these devices where the gate is wrapped around the entire channel. In the off-state bias condition, carrier conduction in GAA is dominated by the volume inversion phenomenon (Munteanu & Autran, 2003): carriers flow from source to drain over the entire silicon film thickness. This is not the case for FinFET devices, where the electron density is not centered in the middle of the film. Figure 5(b) also shows that the electron density in the nanowires situated in the third

stack is very slightly disturbed by the ion strike. Figure 6 also shows that the electron density is strongly enhanced in the first nanowire stack (the impacted stack) after the ion strike (for $t=10$ ps in Fig. 6) and decreases as long as the structure relaxes and the deposited charge is collected or recombined. In the same time, the electron density in the third nanowire stack is almost unchanged compared to the electron density before the ion strike. This confirms the above remarks concerning the variation of the electrostatic potential.

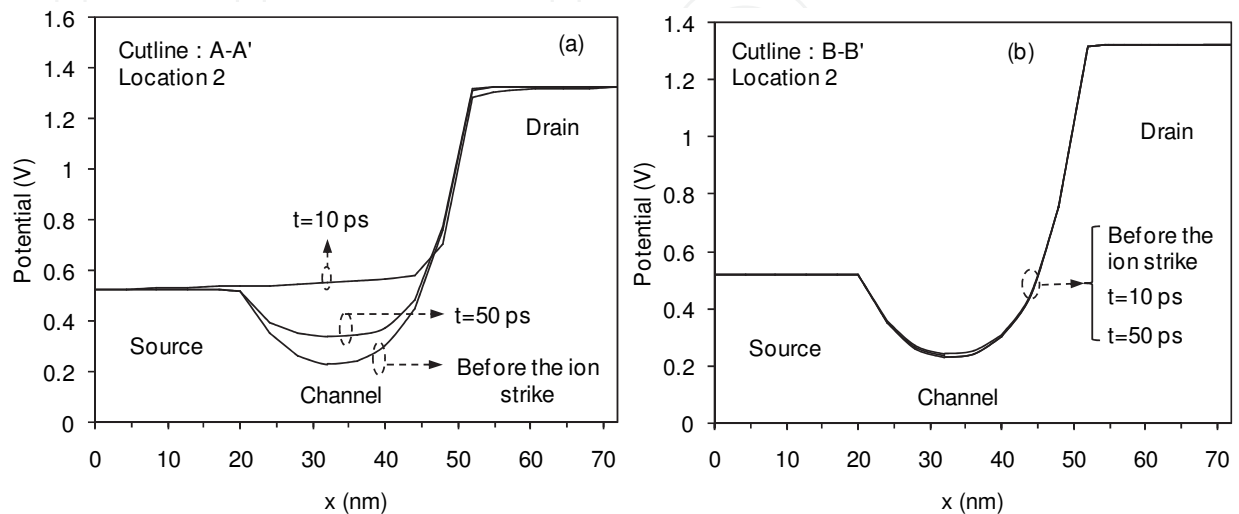


Fig. 5. 1-D potential profiles at different times in two cut-lines (indicated in Fig. 4(a)) along the x-axis in the middle of the nanowire: (a) cutline A-A' in the impacted GAA nanowire and (b) cutline B-B' in the GAA nanowire symmetrically situated in the third stack. The MCFET is biased in the off-state ($V_G=0$ V, $V_D=0.8$ V). The nanowire spacing is $s=100$ nm, the ion strike LET is 10 MeV/(mg/cm²), and the ion track radius is 50 nm.

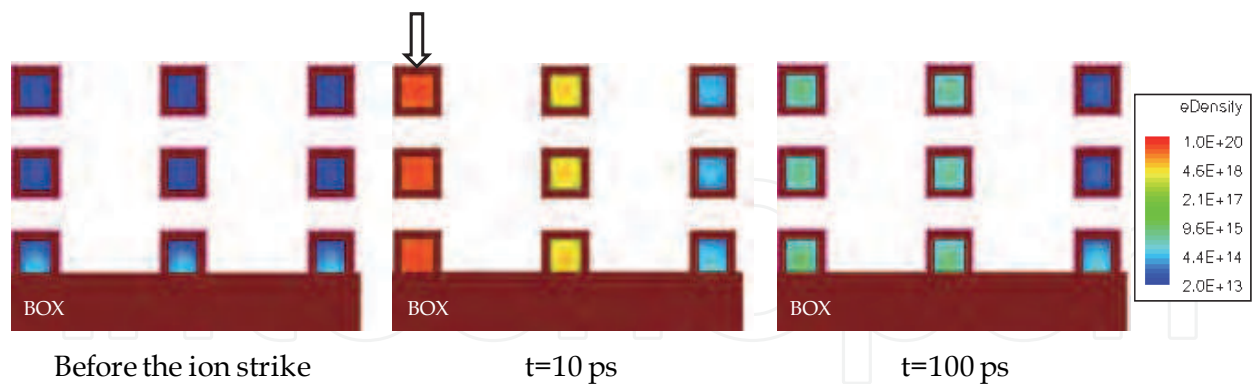


Fig. 6. 2-D profile of electron density along the cross-section C-C' of Fig. 4(b) in the 3D MCFET before the ion strike, at $t=10$ ps and $t=100$ ps. The gate material is not shown. The ion strike location is indicated by the arrow. Other parameters as in Fig. 4.

4.2 Drain current density and charge collection

Figure 7 shows the drain current transient resulting from the ion strike in location "2". The variation of the collected charge with time is also reported. The charge collection is very fast in MCFETs, due to the GAA devices which have small active volumes that allow all the

excess charge to be quickly evacuated. In addition, the GAA architecture allows the floating body-effects to be reduced, due to an excellent control of the body potential by the gate. It has been shown in (Munteanu et al., 2007) that the individual GAA device (with the same geometrical parameters as in the present work) has a total transient duration of 8 ps at 10% of the peak value for LET=10 MeV/(mg/cm²). The single-event transient of the MCFET simulated here has a total transient duration of 10 ps at 10% of the peak value for a LET of 10 MeV/(mg/cm²). This value is lower than that obtained in (Munteanu et al., 2006) for fully-depleted single-gate SOI devices with 50 nm gate length (where a total transient duration of 15 ps at 10% of the peak value is found). However, in (Munteanu et al., 2006) a LET of 30 MeV/(mg/cm²) and a radius of 14 nm have been used. To facilitate the comparison, we considered here a fully-depleted single-gate SOI device having the same geometrical structure as the multiple-gate devices composing the MCFET. For this device, we have simulated the drain current transient for a LET of 10 MeV/(mg/cm²) and a radius of 50 nm. A transient duration of 13.5 ps at 10% of the peak value has been found. The values obtained for MCFET are consistent with transient duration obtained in simulation in (Ferlet-Cavrois et al., 2005), but they are very low compared with those expected by extrapolation from simulations in (Dodd et al., 2004). This is probably due to the partially depleted structures used in (Dodd et al., 2004), whereas ultra-thin fully-depleted devices are considered here.

To resume, simulation results show that MCFET devices exhibit a quick charge collection, faster than that of fully-depleted/partially-depleted SOI devices with similar structure parameters. This short pulse width in MCFET devices could be interesting for single event transient hardening (Diehl et al., 1983; Dodd et al., 2004). From all these results, we could expect that MCFET devices being less sensitive to heavy ion irradiation than fully-depleted/partially-depleted SOI devices. This is mainly due to the excellent immunity to single-event effects of GAA and to the small active volume of individual nanowire devices.

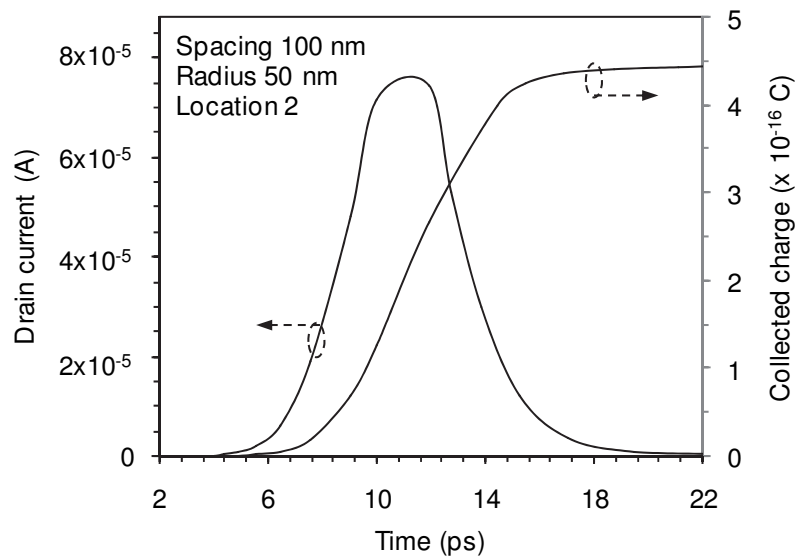


Fig. 7. Drain current transient and collected charge induced by an ion striking in the middle of the silicon film for the ion strike location "2". The MCFET is off-state biased ($V_G=0$ V, $V_D=0.8$ V). The nanowire spacing is $s=100$ nm, the LET value is 10 MeV/(mg/cm²), and the ion track radius is 50 nm.

5. Impact of the ion strike parameters and lateral spacing between nanowires

5.1 Ion strike location and spacing between nanowire stacks

Drain current transients for a vertical ion strike and four ion strike locations are shown in Fig. 8(a) for a MCFET with a lateral spacing $s=100$ nm and an ion track radius of 50 nm. Figure 8(a) shows that for $s=100$ nm the ion striking in locations "2" and "4" produces identical drain current peaks and almost identical drain current transients. These locations correspond to a strike centered in the middle of a silicon nanowire, while locations "3" and "1" correspond to a strike between nanowires, on the isolation oxides. The drain current peak obtained for locations "2" and "4" is higher than that for location "3" which is higher than that for location "1". This is due to the higher deposited charge for locations "2" and "4" than for "3" and "1". These results are consistent with (Alles et al., 2005). It is interesting to note that for the considered lateral spacing ($s=100$ nm), which is large compared to the ion track radius (50 nm), the strikes centered on any nanowire (locations "2" or "4") produces almost the same current transient.

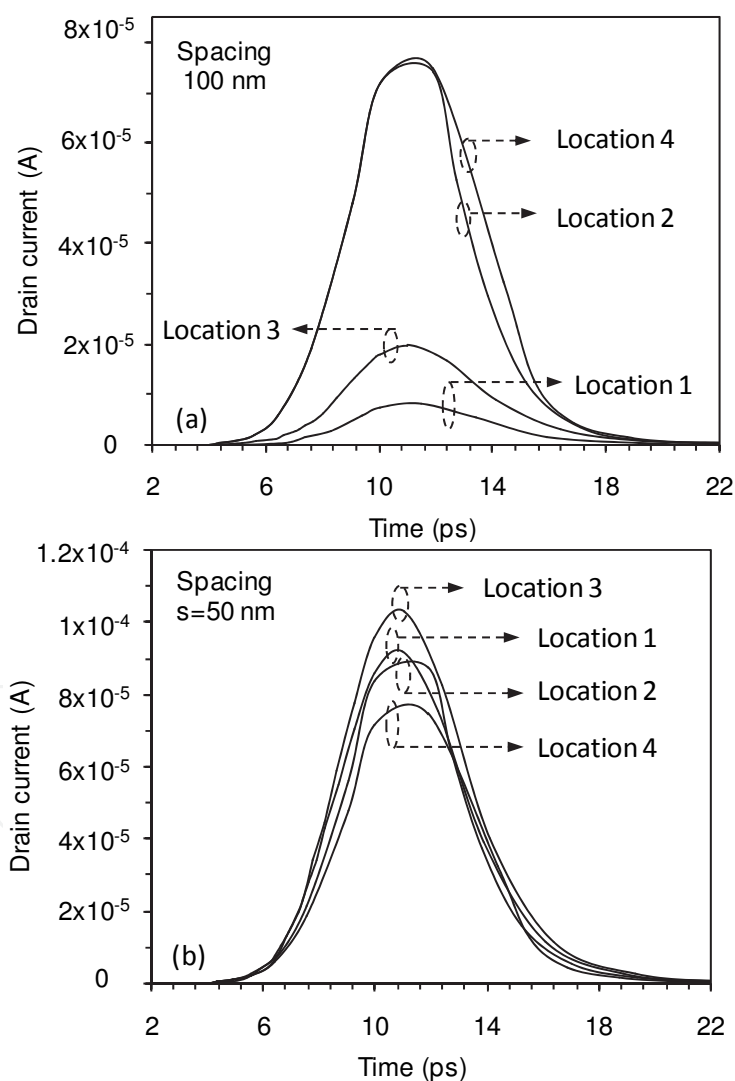


Fig. 8. Drain current transients induced by an ion striking vertically (parallel to y axis) in the middle of the structure. Four strike locations are considered ("1" to "4", as shown in Fig. 2). The MCFET is off-state biased ($V_G=0$ V, $V_D=0.8$ V). The lateral spacing is $s=100$ nm, the ion LET is 10 MeV/(mg/cm²) and the ion track radius is 50 nm.

An interesting analysis concerns the influence on the drain current transient and collected charge of the lateral spacing between the nanowire stacks. Increasing the lateral spacing between nanowires (and keeping constant the ion track radius) will not change the results compared to those obtained for $s=100$ nm. The interesting case is when the lateral spacing is reduced and the ion track radius is kept constant. For a thorough investigation, we simulated two additional MCFET structures having lateral spacings of $s=75$ nm and $s=50$ nm, and we compare the results with those obtained for $s=100$ nm. The drain current transients produced by the ion strike are plotted in Fig. 8(b) for the ion strike locations "1" to "4" and for $s=50$ nm. In these figures the LET value is 10 MeV/(mg/cm²).

We can see that when reducing the lateral spacing from 100 nm to 50 nm, the drain current transients produced by the strikes centered in the middle of the nanowire are no longer identical (the drain transient peak for location "4" becomes lower than for location "2"). For this small spacing between nanowires, the ion strike between the nanowires (ion strike location "3") produces the highest current peak. These results are consistent with those of (Alles et al., 2005).

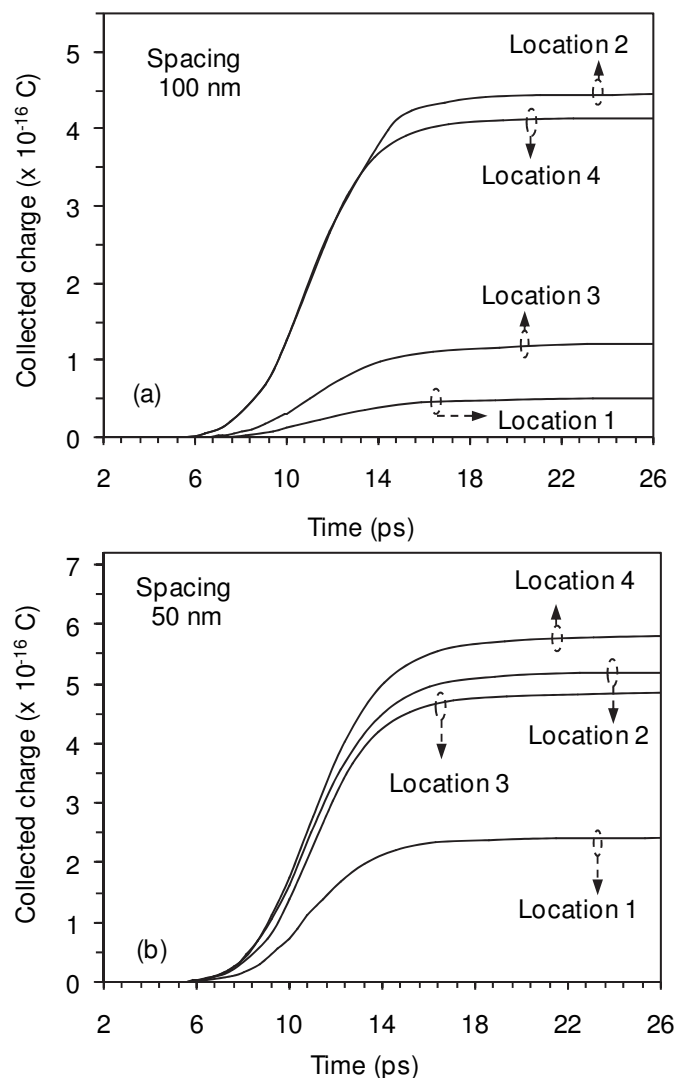


Fig. 9. Collected charge for the drain current transients shown in Fig. 8: (a) $s=100$ nm and (b) $s=50$ nm.

The collected charges extracted as function of time from the drain current transients presented above (Fig. 8) are shown in Fig. 9. For $s=100$ nm (Fig. 9(a)), the collected charge is slightly higher for location "2" than that for location "4". The strikes between nanowires give lower collected charges than the strikes on the silicon nanowires.

When the lateral spacing is reduced to $s=50$ nm (Fig. 9(b)), the collected charge of an ion striking at location "4" becomes higher than those for the other locations. Fig. 9(b) also shows that the collected charge for an ion striking between the silicon nanowires is enhanced when reducing the lateral spacing and becomes closer to that of strikes centered on the nanowire ("2" and "4") for the smallest spacing $s=50$ nm. For a better illustration of this point, we compare in Fig. 10 the drain current transients produced by the ion striking in locations "1" and "3" between the silicon nanowires, for the three lateral spacings (50, 75 and 100 nm). The collected charges corresponding to transients of Fig. 10 are plotted in Fig. 11. Figures 12 and 13 show the drain current transients and the corresponding collected charges for locations "2" and "4" for strikes centered on the nanowire.

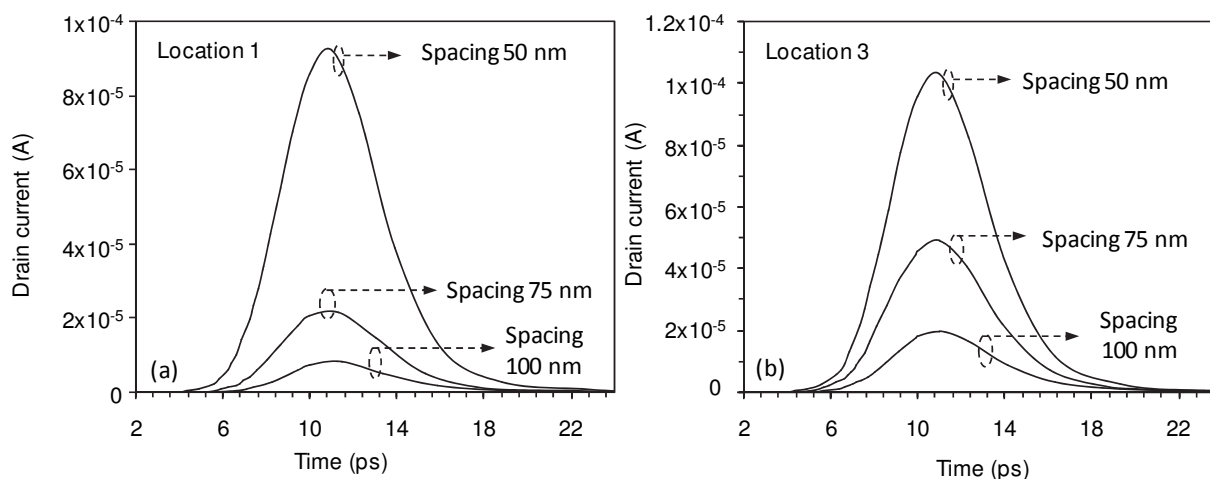


Fig. 10. Drain current transients induced by an ion striking on locations between the silicon nanowire stacks: (a) location "1" and (b) location "3". Three lateral spacings are considered $s=100, 75$ and 50 nm. The MCFET is off-state biased ($V_G=0$ V, $V_D=0.8$ V). The LET value is 10 MeV/(mg/cm²) and the ion track radius is 50 nm.

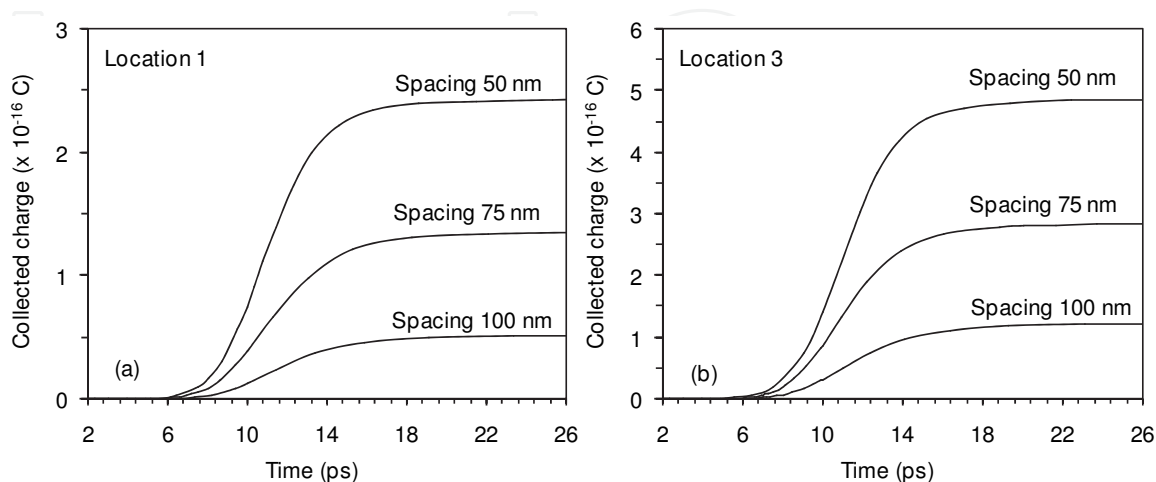


Fig. 11. Collected charge for the drain current transients presented in Fig. 10: (a) location "1" and (b) location "3".

Figures 10(a) and 10(b) indicate that for the locations "1" and "3" strike situated between the nanowires the drain current transients are different for the three lateral spacings. Both the current peak and the collected charge (Figs. 11(a) and 11(b)) increase when the lateral spacing decreases. Figure 12(a) shows that almost the same drain current transient is obtained for the location "2" for large spacing $s=100$ nm and $s=75$ nm. The transient peak is higher for $s=50$ nm than for the larger lateral spacings. For this location, the collected charge decreases when the lateral spacing is increased. For location "4" (Fig. 12(b)) the drain current transient is identical for the three locations; however the collected charge is higher for $s=50$ nm and is the same for $s=75$ nm and 100 nm.

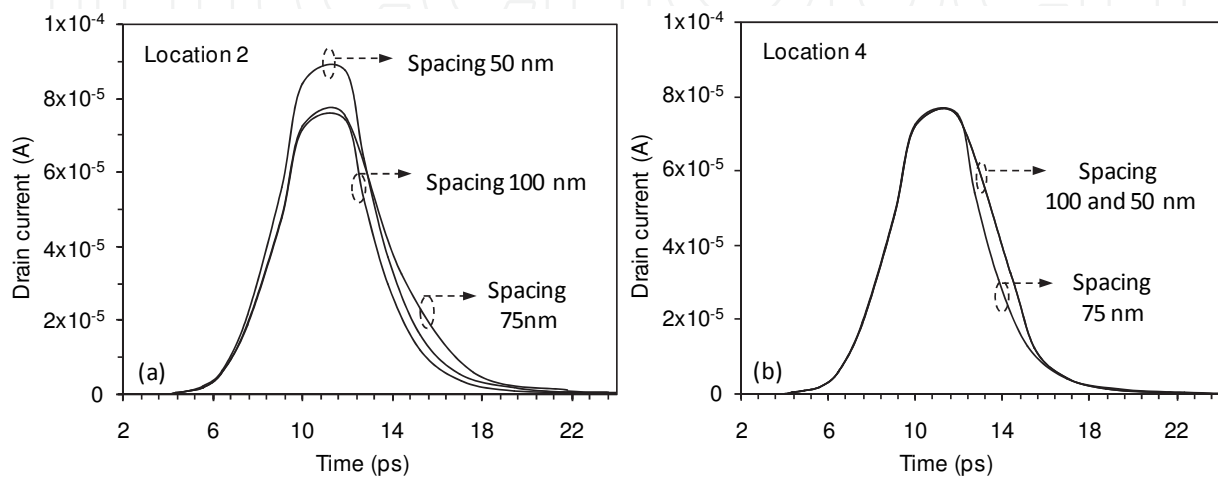


Fig. 12. Drain current transients induced by an ion striking on locations centered on the silicon nanowire: (a) location "2" and (b) location "4". Three lateral spacings are considered $s=100$, 75 and 50 nm. The MCFET is off-state biased ($V_G=0$ V, $V_D=0.8$ V). The LET value is 10 MeV/(mg/cm²) and the ion track radius is 50 nm.

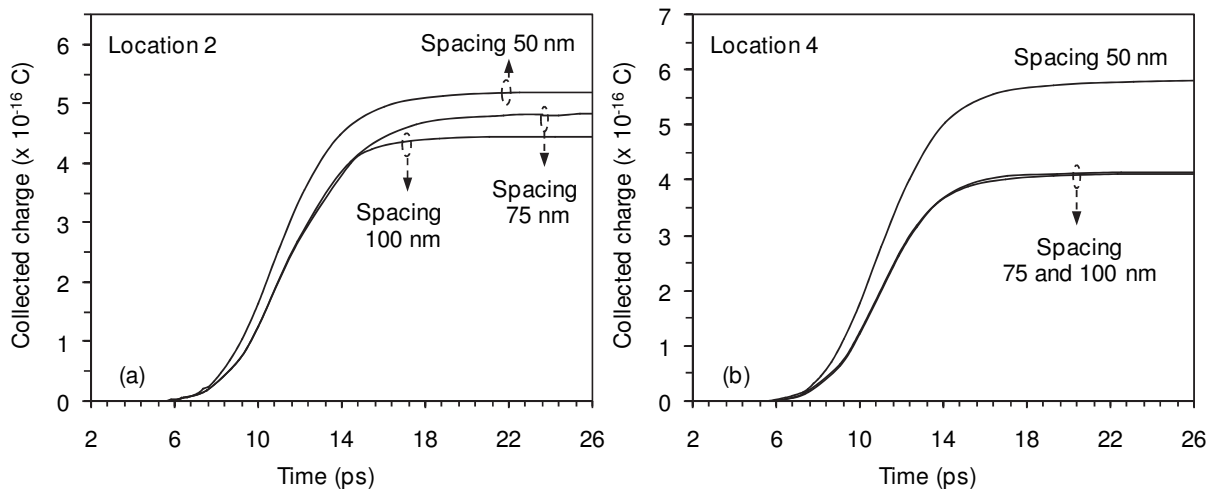


Fig. 13. Collected charge for the drain current transients presented in Fig. 12.

5.2 Ion strike direction and ion track radius

We analyze in this section the impact of the direction of the ion strike and the influence of the ion track radius. The results presented above have been obtained for ion striking

vertically (parallel to y-axis). Then, we have simulated an ion horizontally striking (parallel to the z-axis) on the gate on locations "5", "6", and "7" shown in Fig. 2. Locations "5" and "6" represent a strike in the middle of the silicon GAA nanowire, perpendicular to the gate, while location "7" corresponds to an ion strike on the FinFET device. All these strikes are centered on the silicon nanowire. Figure 14 shows the drain current transients obtained for the three horizontal strikes described above. In this figure, the drain current transient for a vertical strike on location "2" is also reported for comparison. The results show that the transient peaks for horizontal strikes are higher than the peak obtained for a vertical strike on location "2". This is probably due to the higher deposited charge for a horizontal direction due to the large depth of the MCFET device in the z-direction.

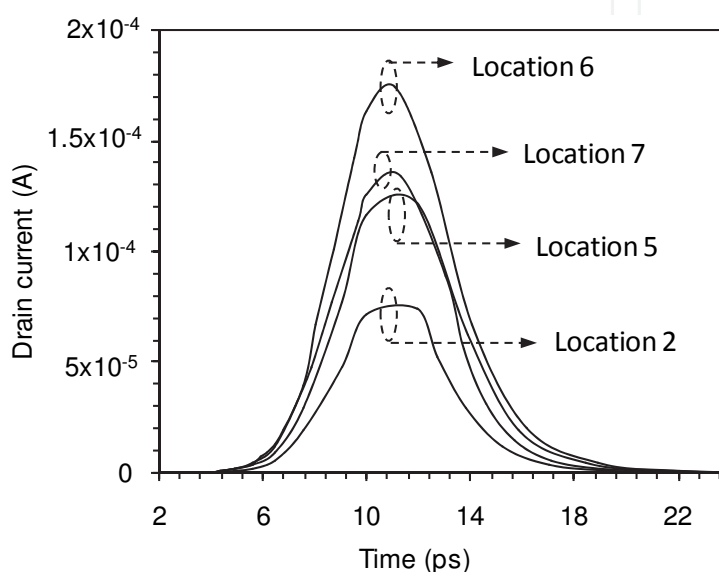


Fig. 14. Drain current transients induced by a horizontal ion strike (parallel to z-axis) in the middle of the silicon film. The drain current transient for a vertical strike on location "2" is also reported. The MCFET is off-state biased ($V_G=0$ V, $V_D=0.8$ V). The LET value is 10 MeV/(mg/cm²), the lateral spacing is $s=100$ nm and the ion track radius is 50 nm.

For the horizontal direction of the ion strike previously considered, an interesting study concerns the impact of the ion track radius. We simulated the ion strike considering two ion track radii, 50 nm and 20 nm. Figure 15(a) shows the drain current transients obtained in these cases for an ion strike in location "6". Drain current transients obtained for ion strikes in locations "5", "6" and "7" for a radius of 20 nm are also shown in Fig. 15(b). The current peak is higher when considering a narrow radius, because more of the charge is localized in the nanowire with the smaller characteristic radius, instead of being generated in the wire-to-wire isolation. This is confirmed in Fig. 16, where the collected charge is plotted for different horizontal strike locations. The collected charge is higher for a 20 nm radius than for a 50 nm radius for the three locations of the ion strike. For a narrow radius ($=20$ nm) the lowest collected charge is obtained for an ion striking on the FinFET device, while for a large radius ($=50$ nm) the strike on the first GAA device of the stack gives the lowest collected charge. The highest charge is obtained for an ion striking the GAA device located in the middle of the vertical stack for both ion track radii considered here.

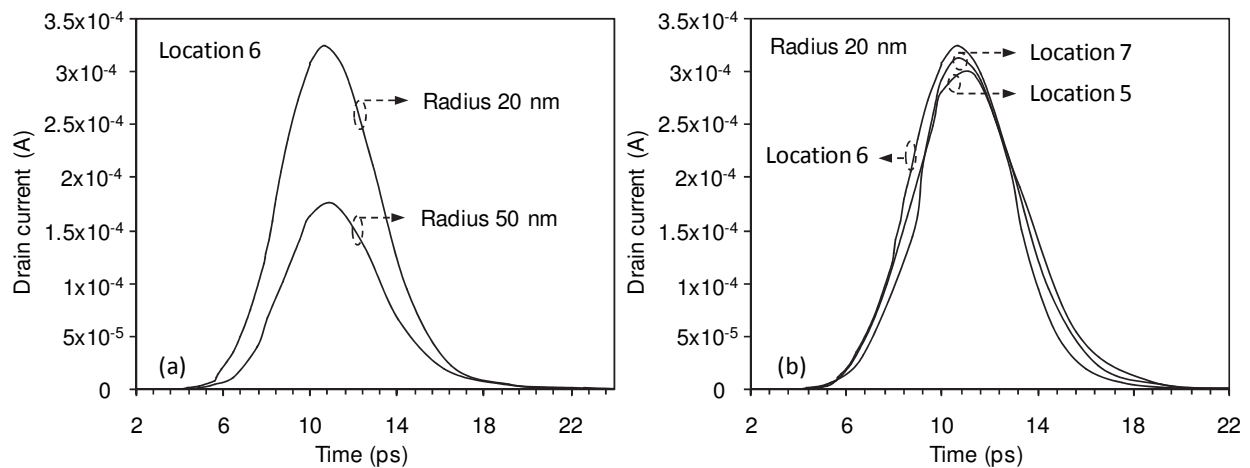


Fig. 15. Drain current transients induced for a horizontal ion strike (parallel to z axis) and two ion track radii. The MCFET is off-state biased ($V_G=0$ V, $V_D=0.8$ V). The LET value is 10 MeV/(mg/cm²) and the lateral spacing between nanowires is $s=100$ nm.

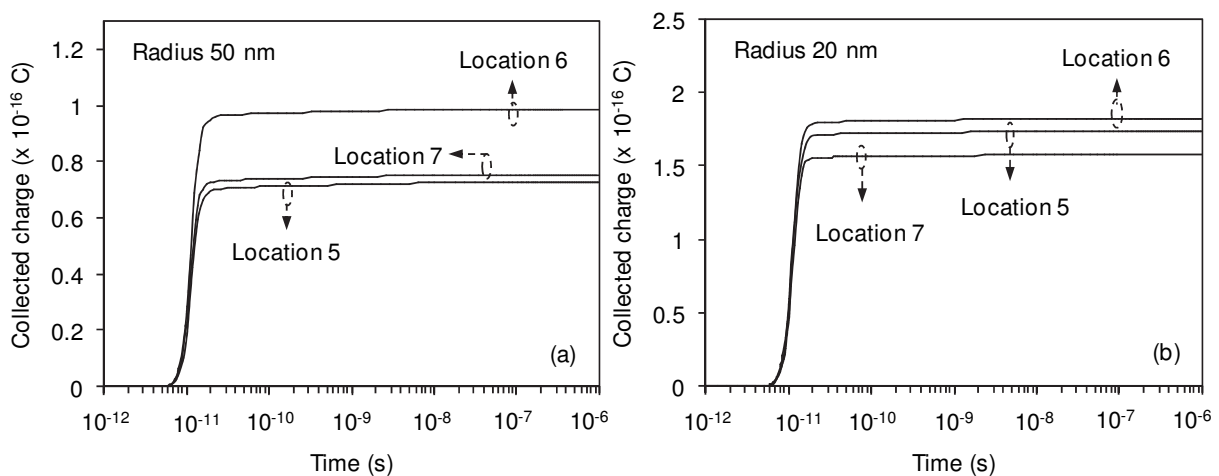


Fig. 16. Collected charge for the drain current transients in Fig. 15.

6. Conclusion

This work investigated the single-event response of 3-D multi-channel nanowire MOSFETs using 3-D numerical simulation. We analyze the evolution in time after the ion strike of both the electrostatic potential and the electron density in the 9 individual devices of the MCFET matrix. We show that the drain current transients and collected charge strongly depend on the ion strike location, direction and track radius. The lateral spacing between adjacent nanowire stacks is found to be a key-parameter in the analysis of the worst case location of the ion strike. We show that for a large lateral spacing between stacks compared with the ion track radius, the strikes centered on any nanowire produces almost the same current transients. In this case the transient peak is higher than that obtained for a strike between nanowires on the isolation oxide. On the contrary, for a small lateral spacing, comparable to the ion track radius, the highest current peak is obtained for a strike between the nanowires.

However, the highest collected charge is obtained for the strike on the nanowire situated on the center of the MCFET matrix. Finally, our results show that the charge collection is very fast in a MCFET for all ion strike parameters and configurations. This is due to the multiple-gate devices which have small active volumes that allow all the excess charge to be quickly evacuated. The MCFET simulated here has a total transient duration of 10 ps at 10% of the peak value for LET=10 MeV/(mg/cm²), which is almost identical to that of a individual GAA device, but lower than that obtained in simulation of fully-depleted single-gate SOI devices. From these results, we could expect a better immunity to single-event phenomena of MCFETs compared to other conventional structures, such as fully-depleted/partially-depleted SOI devices. This will probably have a consequence on the behaviour under irradiation of circuits based on these devices. However, the single device behaviour is not enough to determine the circuit sensitivity to single-events because this also depends on the load capacitance. Since the single-event transients of MCFETs are high-bandwidth, they are very sensitive to inductive and reactive capacitance (i.e., node loading) in the circuit. More detailed study concerning this point is needed to exactly quantify the sensitivity to single-event of MCFETs-based circuits.

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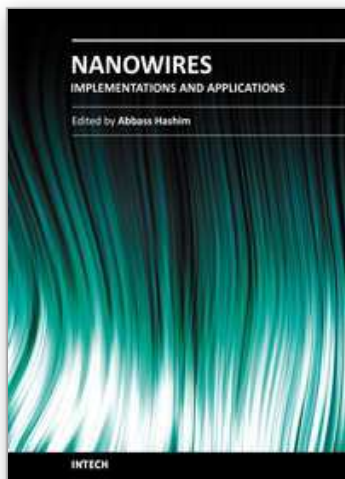
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